Microelectronics Journal 102 (2020) 104801

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Dynamic differential signaling based logic families for robust ultra-low power near-threshold computing

MD Shazzad Hossain *, Ioannis Savidis

Drexel University, Philadelphia, PA, USA

ARTICLE INFO

Keywords:
Near-threshold computing
Low power circuits
Dynamic differential signaling based logic
Current mode logic
Robustness to noise and variation

ABSTRACT

In this paper, novel circuit topologies for near-threshold computing (NTC) are proposed and evaluated. Three separate dynamic differential signaling based logic (DDSL) families are developed in a 130 nm technology to operate at 400 mV and 450 mV. The proposed logic families outperform contemporary CMOS and current-mode logic (CML) circuits implemented for near-threshold. The DDSL families are described as dynamic current-mode logic (DCML), latched DCML (LDCML), and dynamic feedback current-mode logic (DFCML). Simulation and analysis are performed through implementation of boolean functions and a 4×4 bit array multiplier. At a 450 mV supply voltage, the total power of the 4×4 DFCML multiplier is reduced to 0.95× and 0.009×, while the maximum operating frequency is improved by 1.4× and 1.12× as compared to, respectively, a CMOS and CML multiplier. The DCML multiplier consumes 1.48× the power while improving f_{max} by 1.65× as compared to a CMOS multiplier. A chain of four inverters implemented with the developed dynamic logic families exhibited an energy delay product (EDP) of 0.27× and 0.016× that of, respectively, CMOS and CML implementations. The mean noise margins, also evaluated with a chain of inverters, of DFCML and LDCML are at least 2.5× greater than that of CMOS.

1. Introduction

Among the many ultra-low power techniques available at the circuit, architecture, and system level including dynamic voltage scaling, dynamic voltage and frequency scaling, power gating, clock gating, and charge recycling [8], supply voltage scaling is the most effective. Therefore, near-threshold computing (NTC), where the supply voltage is set close to the threshold voltage of the transistors, is an effective technique for applications with moderate performance requirements as NTC provides the optimum energy-performance trade-off [1–7]. The dynamic power consumption is linearly dependent on the activity factor α, load capacitance C_L, and clock frequency f_{clock}, while quadratically dependent on the voltage as given by (1), where V_{dd} is the supply voltage and $V_{switching}$ is the output voltage swing (often the same as V_{dd}) [9–11]. In addition, the scaling of the supply voltage increases the gain of a CMOS inverter as given by (2) [12], where r is the relative drive strength of the PMOS and NMOS transistors (r is set to 1 for a symmetric inverter), V_M is the switching threshold of a CMOS inverter, and λ_n and λ_p are the channel length modulation terms for, respectively, an NMOS and PMOS transistor due to short-channel effects. Scaling the supply voltage close to the value of the threshold voltage, therefore, optimizes the energy efficiency of the circuit without significantly impacting the maximum clock frequency as compared to the resulting sharp decrease in frequency when operating in sub-threshold, as shown in Fig. 1.

$$P_{dynamic} = \alpha \cdot f_{clock} \cdot V_{dd} \cdot V_{switching} \cdot C_L \tag{1}$$

$$gain = \frac{1+r}{(V_M - V_{Tn} - \frac{V_{DSATn}}{2})(\lambda_n - \lambda_p)} \tag{2}$$

$$V_M = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{dd} + V_{Tp} + \frac{V_{DSATp}}{2})}{1+r} \tag{3}$$

Three operating regions are described based on the set supply voltage of the circuit as compared to the threshold voltage of the transistors: 1) *Super-threshold* (super-V_t), where the supply voltage is considerably higher than the threshold voltage, 2) *near-threshold* (near-V_t), where the supply voltage is equal to or slightly above the threshold voltage of the transistors, and 3) *sub-threshold* (sub-V_t), where the supply voltage is less than the threshold voltage of the transistors [6]. Researchers have worked to exploit the potential of sub-V_t circuits for the past three

* Corresponding author.
E-mail address: msh89@drexel.edu (M.S. Hossain).

https://doi.org/10.1016/j.mejo.2020.104801
Received 6 January 2020; Received in revised form 30 March 2020; Accepted 21 April 2020
Available online 1 May 2020

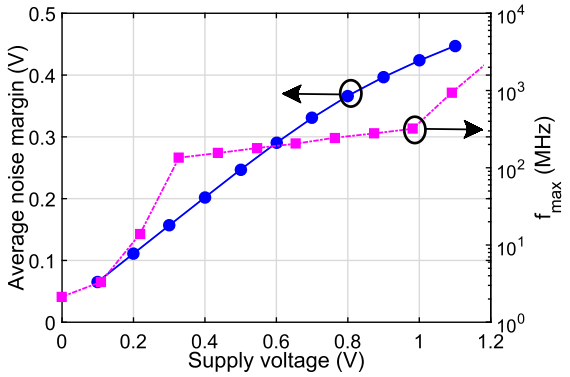


Fig. 1. Effects of supply voltage scaling on the maximum operating frequency and average noise margins of a CMOS inverter with a PMOS width of 5.77 μm and a NMOS width of 2 μm in a 130 nm technology.

decades, where 36 mV was determined as the theoretical lower limit of the supply voltage that permitted transistor activity [6,13]. There are, however, critical constraints with sub-V_t circuits such as increased functional failure [6], increased sensitivity to process, voltage, and temperature (PVT) variation [14], and an exponential dependence of the current (leakage current in sub-V_t) on the scaled supply voltage [15,16]. In addition, sub-V_t circuits incur a severe degradation in performance as there exists an exponential relationship between the supply voltage and the maximum operating frequency, as shown in Fig. 1 [6,14]. Near-threshold circuits, however, provide an optimum trade-off between energy efficiency and performance, while also maintaining a moderate noise margin as compared to super-V_t and sub-V_t circuits [5,6]. Therefore, near-V_t circuits have gained traction in the research community [1–7,10,11,17–20].

Circuits utilizing differential input and output signaling are well suited for high-speed and robust operation as compared to traditional single-ended logic such as CMOS and dual mode based logic families [21–23]. CMOS based logic suffers from inherent limitations at low supply voltages, which include performance degradation, reduced noise margins (as shown in Fig. 1), and lower voltage swing at the output of a gate [2,5–7,17,19,20]. The output voltage swing is as equally important as the supply voltage to reduce the dynamic power consumption of a circuit, as given by (1). The use of differential signaling provides a larger swing in the output voltage of the gate as compared to single ended logic including CMOS and dual mode logic, which is beneficial for both low voltage and high performance applications as the delay and switching power are reduced [7,21,24–29]. Prior work characterizing logic circuits operating at near-V_t voltages with differential input and output signaling was performed and compared to standard CMOS implementations [30]. Circuits based on MOS current-mode logic (MCML) and sense-amplifier based logic (SAPTL) were proposed for NTC [6,7,24,31]. The primary drawback of current-mode and sense amplifier based logic, however, is the static current path through the tail transistor, which results in a significant increase in the power consumption [6,24,32]. As large transistors are required to maintain the static current through the gate, the capacitive load and, therefore, the delay increases. In addition, the robustness to noise and the energy efficiency of both circuit families operating at low frequencies and at scaled supply voltages is not analyzed.

The differential cascode voltage switch logic (DCVSL) gate and modified variants have been implemented for high performance circuits operating at super-V_t supply voltages [27–29,33–35]. However, the analysis of DCVSL-type circuits operating at sub- and near-V_t voltages has not been explored [27–29,33–35].

In this paper, three novel dynamic differential signaling based logic (DDSL) families are developed and characterized for NTC that are robust to noise and variability. The three DDSL families are proposed to address the limitations of CMOS and CML circuits operating at near-V_t voltages.

The primary contributions of this paper include:

1) the development and characterization of a novel pseudo-differential based logic family (DFCML) for NTC,
2) the development of two differential signaling based DCVSL-type logic circuits (DCML and LDCML) for NTC,
3) a method to determine the noise margins of differential signal based logic circuits, and
4) the generation of a closed-form expression of the gain of a DCML inverter.

The potential applications of the DDSL families for NTC include battery operated ultra-low voltage devices such as arithmetic units of hardware inference accelerators for edge AI applications, energy-efficient and low-performance sub-circuits of an SoC, implantable medical devices, health monitoring systems, sensory networks, and wearable devices. The rest of the paper is organized as follows: The three DDSL families are described in Section 2. Implementation of boolean functions and a 4×4 bit array multiplier with each logic family is described in Section 3. The simulated results characterizing each logic family are provided in Section 4. Concluding remarks are provided in Section 5.

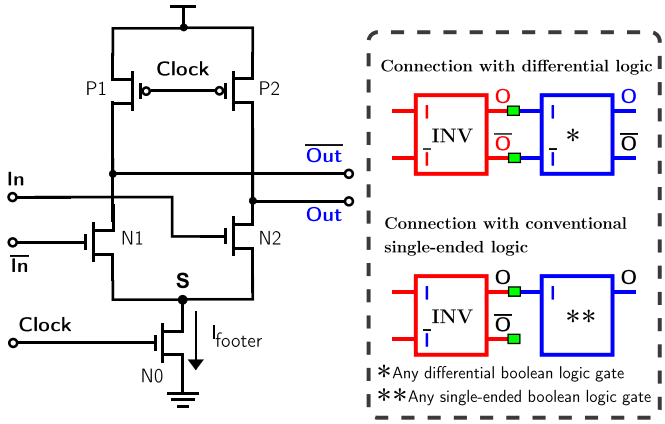
2. Dynamic differential signaling based logic families

While supply voltage scaling improves energy efficiency, the challenge is to achieve low voltage operation without significantly impacting the performance and robustness of the circuit. In this work, robust logic families are proposed for NTC that function at low voltage while improving the performance and the robustness to noise as compared to CMOS and CML implementations. The DDSL circuits mitigate energy loss due to the static current path through the footer transistor of CML gates by operating in two phases: ***1) pre-charge***, and ***2) evaluate***. As the charging and discharging paths never turn on simultaneously, when assuming that no clock skew exists in the clock network, the two phase operation of DDSL circuits also reduces the short-circuit current, which is more pronounced in conventional CMOS circuits operating at near-threshold. Both the delay and power consumption of DDSL circuits are, therefore, reduced at near-V_t operating voltages [12].

In order to benefit from the increased operating frequency, reduced power consumption, and greater robustness to noise provided by DDSL, a family of three logic circuits are developed and characterized for NTC: 1) dynamic current mode logic (DCML) described in Section 2.1, 2) latched DCML (LDCML) described in Section 2.2, and 3) dynamic feedback current-mode logic (DFCML) described in Section 2.3. The implemented DCML and LDCML families are based on a DCVSL gate [27–29], while the DFCML family is based on a static FCML gate [36]. The implemented logic families are described as *dynamic* and *current-mode* since functional principles of both dynamic and current-mode logic circuits apply [30]. The DDSL families differ in the structure of the pull-up network (PMOS devices) and the two differential branches. However, the fundamental operation of all DDSL circuits is similar.

2.1. Dynamic current mode logic (DCML)

The schematic of a DCML inverter is shown in Fig. 2. Unlike conventional CMOS gates, the circuit operation is controlled by two identical differential current paths. In addition, the current I_{footer} through the gate is regulated by an applied voltage on the footer transistor *N0*, which affects the input voltage and operating characteristics of the next stage. During the pre-charge phase, both the *Out* and $\overline{Out}$ nodes are charged to V_{dd} and the entire circuit is disconnected from the V_{gnd} node. During the evaluate phase, depending on the signals on *In* and $\overline{In}$, *Out* or $\overline{Out}$ is discharged through, respectively, transistor *N2* or *N1*.



	In	$\overline{In}$	Input	Out	$\overline{Out}$	Output
State 1	0	1	0	1	0	1
State 2	1	0	1	0	1	0

Fig. 2. Implementation of an inverter with dynamic current-mode logic (DCML). The differential logical operation of the DCML inverter is provided in the table. The output of a DCML inverter is connected to inputs of either a single-ended or differential signal based logic gate as shown by the sub-figure in the dotted box.

The logical evaluation of the inverter is provided in the table included as part of Fig. 2. The voltage difference between *In* and $\overline{In}$ defines the ***Input*** (V_{In} - $\overline{V_{In}}$) of the logic gate, while the difference between *Out* and $\overline{Out}$ defines the ***Output*** (V_{Out} - $\overline{V_{Out}}$). In order to evaluate the functionality of a DCML inverter, V_{dd} is applied to the *In* port (V_{In}) and V_{gnd} to the $\overline{In}$ port ($\overline{V_{In}}$). The voltage difference between *In* and $\overline{In}$ is $V_{dd} - V_{gnd} = V_{dd}$, which is evaluated as logic high. During the evaluation phase, *Out* discharges through *N2* and the $\overline{Out}$ node remains high. If the output is taken as the difference between *Out* and $\overline{Out}$, the resulting -V_{dd} is evaluated as logic low, and the input signal is inverted. If, however, the output is evaluated as the difference between $\overline{Out}$ and *Out*, the circuit behaves as a buffer. Explicit inversion is, therefore, not required for dynamic current-mode logic.

The input-output characteristics of the DCML inverter are described by the voltage transfer curve (VTC) shown in Fig. 3. The points where the derivative of the VTC curve is −1 are labeled as *A* and *B*. The differential voltage of the output to the left of point *A* represents logic high, and the voltage of the output to the right of *B* represents logic low. As *In* is increased with respect to $\overline{In}$, more current flows through branch 2 as compared to branch 1, which results in a decrease in the voltage at *Out*, while $\overline{Out}$ remains unchanged. As a result, the differential ***Input*** and ***Output*** voltage of the logic circuit begins to increase and decrease, respectively.

A chain of inverters is used to evaluate the self restoring property and drive capability of the DCML inverter and to characterize the delay for a rising and falling output voltage of the logic families. The overdrive voltage V_{od} given by (4) [37] is an important parameter used to regulate the output voltage swing. Depending on the voltages at the terminals and the transistor dimensions, the overdrive voltage varies between 20 to 120 mV and 0 to 100 mV for, respectively, the PMOS and NMOS transistors of a 130 nm CMOS process. Assuming a set supply voltage, and therefore, gate voltage, modifying the width is the most effective means to set the overdrive voltage of the transistors. However, increasing the width results in a larger intrinsic load capacitance, which produces a longer propagation delay. There is, therefore, a trade-off and upper limit between reducing the power consumption and preserving the performance when modifying the transistor width.

$$V_{od} = (V_{GS} - V_T) = \sqrt{\frac{2I_{footer}}{\mu_n C_{ox}\frac{W}{L}}} \tag{4}$$

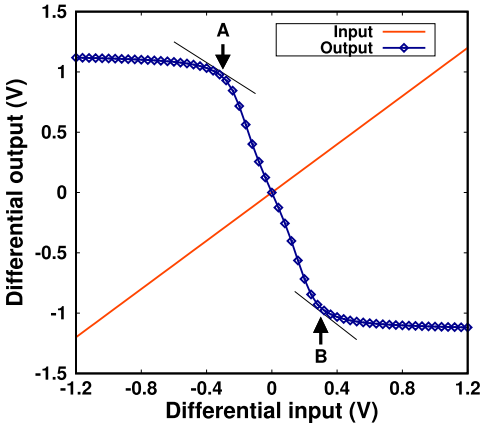


Fig. 3. Voltage transfer curve of a differential inverter for a V_{dd} of 1.2 V.

Assuming that a single clock signal is distributed throughout the circuit, a chain of DCML gates lacks the self-restoring property due to a floating state in the evaluation phase. As a result, within a given clock cycle, the circuit does not evaluate correctly after a certain number of sequentially connected logical stages as the stored charge at the differential output node gradually leaks. For the chain of CMOS inverters operating at a near-V_t supply voltage of 400 mV, including more than four logical stages of CMOS gates is a challenge even with transistors that are sized 5× larger as the full voltage swing is not obtained at the output within the user specified limit of 85% of the input signal period, which is used to determine the maximum operating frequency of the inverter chain. However, at a 400 mV supply voltage and a 1 MHz operating frequency, a chain of DCML inverters functions properly with up to eight sequentially connected logical stages. The logical output is discernible with the use of differential signals, even with a 20 to 30 mV reduction in the voltage swing. At near-V_t operating voltages, a larger number of stages is, therefore, feasible with DCML logic families at a cost of reduced frequency.

2.1.1. Gain of DCML inverters in near-threshold

The gain of a DCML inverter is a function of the supply voltage, threshold voltage, and process parameters. The conventional CMOS dynamic logic inverter exhibits the maximum gain when the voltage of the output node is close to the threshold voltage of the inverter [38]. The voltage at both output nodes of the DCML inverter shown in Fig. 2 is V_{dd} at the beginning of the evaluate phase. Therefore, the current of an NMOS transistor operating in the linear region, as given by (5), is considered. The current through transistors N1 and N2 is, respectively, I_1 and I_2. The total current through the footer transistor I_{footer} is the sum of the currents I_1 and I_2.

$$I_D(linear) = \mu C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{5}$$

$$V_{diff,out} = |V_{Out} - V_{\overline{Out}}| \tag{6}$$

$$\begin{aligned} &= \left(V_{dd} - I_2 \cdot (R_{N2} + R_{N0})\right) - V_{dd} \\ &= I_2 \cdot (R_{N2} + R_{N0}) \\ &= I_{footer} \cdot (R_{N2} + R_{N0}) \end{aligned} \tag{7}$$

$$\begin{aligned} V_{diff,in} &= V_{In} - V_{\overline{In}} \\ &= (V_{dd} - V_{gnd}) \\ &= V_{dd} \\ &= V_{od} + V_T \end{aligned} \tag{8}$$

The differential output voltage is given by (6), where at the end of the pre-charge phase, the voltages at nodes *Out* and $\overline{Out}$ are, respectively, $V_{dd} - I_2(R_{N2} + R_{N0})$ and V_{dd}. When applying a differential input of V_{dd} and V_{gnd} for, respectively, *In* and $\overline{In}$, the charge on *Out* begins to discharge through N2 and N0, which results in a $V_{diff,out}$ as given by (7). The channel ON resistance of NMOS transistors *N*1 and *N*2 is, respectively, R_{N1} and R_{N2}. In addition, $R_{N0} = y \cdot R_{N1} = y \cdot R_{N2}$ as $R_{N1} = R_{N2}$ since both *N*1 and *N*2 are set to the same width and length. The variable *y* represents the ratio of the width of either transistor *N*1 or *N*2 to the width of the footer transistor *N*0 ($y = \frac{W_{N1}}{W_{N0}} = \frac{W_{N2}}{W_{N0}}$). For *In* and $\overline{In}$ set to, respectively, V_{dd} and V_{gnd}, the resulting differential input is, therefore, given by (8).

The maximum gain of the DCML inverter, as given by (9), is calculated using (7) and (8). The gain is further expanded by substituting into (9) the equation of the channel ON resistance $R_N = \frac{1}{\mu_n C_{ox}(V_{GSn}-V_{Tn})\frac{W_n}{L_n}}$ and the equation of the current I_{footer} through *N*0, which results in (10). The variable *m* in (10) is defined as the ratio of the drain voltage V_{DS} to the overdrive voltage $V_{od} = (V_{GS} - V_T)$ and is a value between 0 and 1. Note that the gain is primarily dependent on the threshold voltage, supply voltage, the ratio of the ON resistance of *N*0 to *N*2 or *N*1, and the ratio of drain voltage to the overdrive voltage.

$$gain = \frac{I_{footer} \cdot (R_{N2} + R_{N0})}{V_{dd}} = \frac{R_{N2}(1+y)\mu_n C_{ox} W \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]}{L \cdot V_{dd}} \quad (9)$$

$$gain = \frac{(V_{GS} - V_T) \cdot (1+y) \cdot \left(m - \frac{m^2}{2}\right)}{V_{dd}} = \frac{V_{od} \cdot (1+y) \cdot \left(m - \frac{m^2}{2}\right)}{V_{dd}} \quad (10)$$

2.2. Latched dynamic current mode logic (LDCML)

The LDCML circuits function similar to the DCML circuits, as both operate in two phases. However, the LDCML inverter includes two minimum sized PMOS transistors (P3 and P4) used as keepers, as shown in Fig. 4 [23]. The keeper transistors preserve the output voltage during the evaluation phase if charge leaks at either of the two output nodes. The LDCML logic family, therefore, provides the self-restoring property for a larger number of logical stages, in contrast to DCML circuits. As the keepers prevent voltage drop or charge loss at the output nodes, the circuit is robust to external noise. Aside from leakage current, the P3 and P4 transistors do not consume additional power as there is no direct current path through P3/N1 or P4/N2 (either N1 or N2 is off). In addition, the area overhead is negligible as minimum sized transistors are used.

For the LDCML inverter, once the input signals are applied, there is a hysteresis in the voltage transfer curve due to the keeper transistors *P*3 and *P*4. For example, the voltage difference between *In* and $\overline{In}$ has to be sufficiently large (approximately 180 mV) to flip the potentials of *Out* and $\overline{Out}$ from the previously held values. Since the *Out* node was at a voltage of 450 mV for the previous input conditions, *N*2 must sink enough current to overcome the current supplied by the keeper (*P*4) and discharge the *Out* terminal. As a result, the potential at the gates of *P*3 and *P*4 are also flipped. The hysteresis response of LDCML gates results in improved noise margins for a given differential input.

2.3. Dynamic feedback current mode logic (DFCML)

The DFCML family performs pseudo differential operation, as a single ended input *In* results in a differential output *Out* and $\overline{Out}$, as shown in Fig. 5(a). The transistors *N*1 and *N*2 are controlled by, respectively,

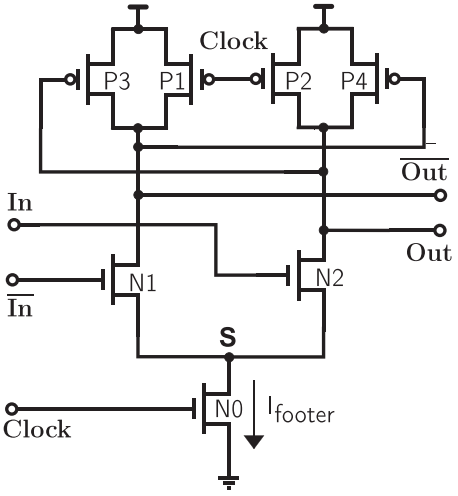


Fig. 4. Implementation of an inverter with latched DCML.

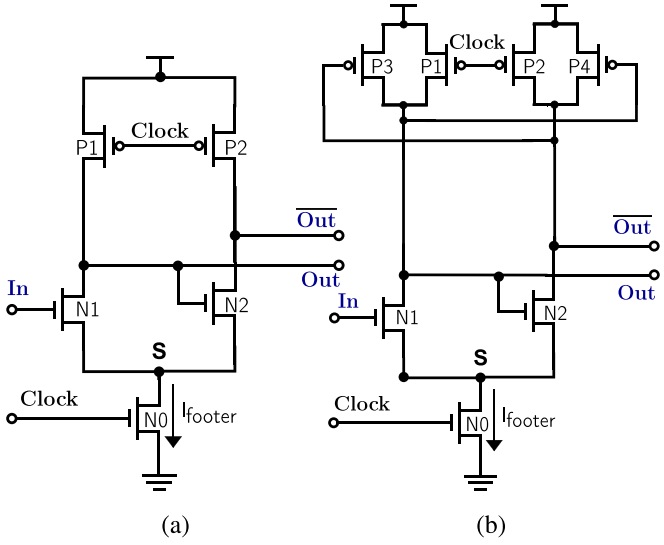


Fig. 5. Implementation of an inverter with a) dynamic feedback current-mode logic (DFCML) and b) latched DFCML (LDFCML).

the input signal and the feedback signal from one of the differential output nodes.

The DFCML circuits follow the operating principles of both dynamic logic and feedback current mode logic (FCML), which was introduced for circuits operating at super-V_t supply voltages [36]. Despite having higher noise immunity and less sensitivity to both parasitic impedances and to process, voltage, and temperature (PVT) variations, FCML circuits sink a significant amount of current due to the static current path through the tail transistor. The energy efficiency is, therefore, improved with DFCML circuits as there is no longer a static current path through the footer transistor, while also providing the improved performance, low voltage of operation, and higher noise immunity offered by FCML. The operation of DFCML circuits is similar to DCML and LDCML circuits as there is both a pre-charge and evaluate phase. However, the proper sizing of the input transistor (*N*1) and the feedback transistor (*N*2) is critical for the proper operation of the DFCML circuits. As both the output nodes are precharged to V_{dd}, *N*1 must be sufficiently large to discharge the *Out* terminal quickly enough to assure that *N*2 turns off and prevents charge sinking from $\overline{Out}$. For the DFCML inverter, the input transistor *N*1 is approximately nine times larger than the feedback transistor *N*2.

A latched DFCML (LDFCML) circuit is also characterized, with a topological structure as shown in Fig. 5(b). With LDFCML, the transistor count is less than LDCML when the gate includes more than one input, which results in lower area and power consumption. Despite the pseudo differential operation, LDFCML benefits from a higher immunity to external noise, less sensitivity to parametric variation, and low voltage operation, similar to a fully differential inverter.

3. Implementation of boolean functions and a multiplier

In addition to inverters, boolean functions including the AND, NAND, NOR, and OR and a 4×4 bit array multiplier are implemented in each DDSL circuit family for operation at near-V_t supply voltages. The implementation of universal gates is presented in Section 3.1, while the multiplier is described in Section 3.2.

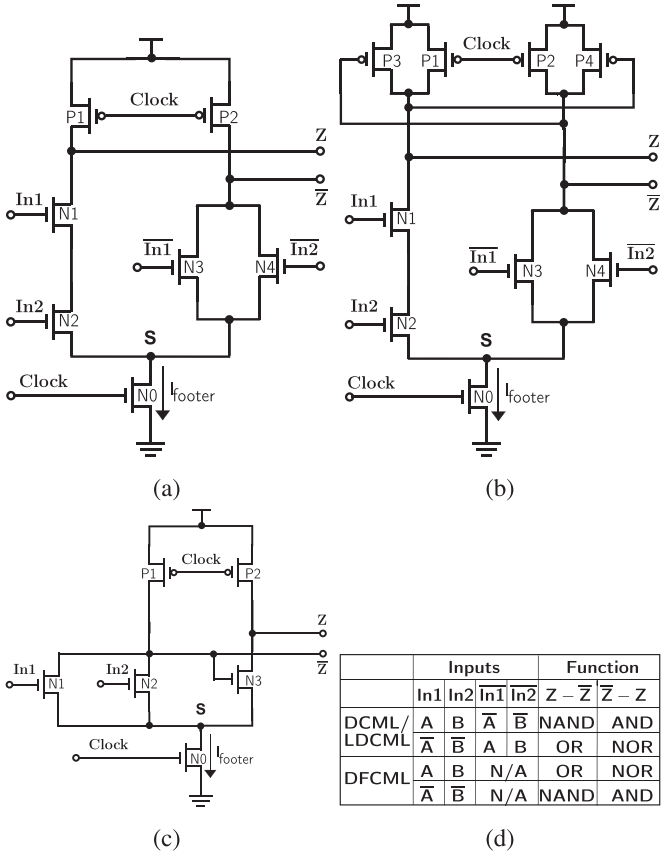
3.1. Universal gates

Dynamic differential signaling based logic (DDSL) circuits allow for a single topology to function as an AND, NAND, OR, or NOR based on the configuration of both the inputs and outputs of the gate. The circuit is, therefore, described as a universal gate (UG). Characterization of the proposed logic families, including when implemented as universal gates, provides an analysis of the benefits and challenges of realizing DDSL circuits. In this work, two input universal gates are implemented using the DCML, LDCML, and DFCML families as shown in Fig. 6, where each gate realizes up to four boolean functions. The circuit operation of the DCML, LDCML, and DFCML universal gates is similar to the operation of, respectively, the DCML, LDCML, and DFCML inverters discussed in Section 2. The proposed gate topologies are compared with CMOS NAND and NOR gates and CML universal gates. As a single DDSL circuit implements four logical functions, the design complexity, design time, and cost of a digital logic circuit is reduced. In addition, unlike standard CMOS, it is not necessary to invert the output of a NAND or NOR gate to implement, respectively, an AND or OR gate. Therefore, the use of the DDSL families results in a reduction in the area, power consumption, and delay as compared to CMOS gates.

Additional transistors are not required in the charging path (the pull-up network) when increasing the number of inputs. However, like CMOS NAND and NOR gates, two MOS transistors are required for each additional input included in DCML and LDCML gates. Therefore, there is a limit in the maximum number of inputs permitted within a gate for a target current and performance requirement as the voltage headroom is reduced when increasing the number of NMOS transistors in series. In order to maintain proper functionality, a minimum DC voltage difference of approximately 200 mV (worst case among all differential logic families) is required between A and $\overline{A}$ and B and $\overline{B}$. Since the DDSL circuits are operating at near-V_t voltages, the voltage headroom is an important parameter that must be met to maintain a proper drain to source voltage (V_{DS}) bias. In this work, no significant drop in voltage headroom is observed for gates with *two inputs*. Unlike DCML and LDCML gates, the DFCML universal gate does not experience a reduction in the voltage headroom as the number of input signals increases, since each additional input is added in parallel to existing inputs that are directly connected to the tail transistor as shown in Fig. 6(c).

3.2. Multiplier implementation

A 4×4 bit array multiplier, which includes 16 AND gates, 4 half adders, and 8 full adders, operating at a supply voltage of 450 mV is implemented in each logic family to characterize the worst-case delay and power consumption. An array multiplier incurs a longer critical path delay and consumes a greater amount of power as compared to other multipliers such as the carry-save multiplier, the wallace-tree multiplier, and the booth multiplier [12]. The propagation delay is measured on the critical path, which is between the least significant bit of one of the inputs and the most significant bit of the multiplier output [12]. The multipliers are implemented using the previously described inverters and universal gates as well as half adders and full adders designed in each logic family. The interconnect between differential signal based logic gates is similar to the method shown for a DCML inverter in Fig. 2.



	Inputs				Function	
	In1	In2	$\overline{In1}$	$\overline{In2}$	Z – $\overline{Z}$	$\overline{Z}$ – Z
DCML/ LDCML	A	B	$\overline{A}$	$\overline{B}$	NAND	AND
	$\overline{A}$	$\overline{B}$	A	B	OR	NOR
DFCML	A	B	N/A		OR	NOR
	$\overline{A}$	$\overline{B}$	N/A		NAND	AND

Fig. 6. Implementation of universal gates using a) dynamic current-mode logic (DCML), b) latched DCML (LDCML), c) dynamic feedback current-mode logic (DFCML), and d) the implementation of four logical functions using two different input and output combinations.

For the CMOS multiplier, 24 additional buffers are implemented to assure full-swing at the outputs. An additional 24 and 14 buffers are needed between the logic gates of the multipliers implemented with, respectively, DCML and DFCML to restore full logical swing as discussed in Section 2.1. However, no additional buffers are needed for the CML and LDCML multipliers. The 14 buffers required for the DFCML multiplier compensate for the larger resistance on one of the discharging paths of each gate, which include transistors of smaller size.

4. Simulation results

The power consumption, maximum operating frequency, and area are characterized through SPICE simulation of implemented boolean functions and a 4×4 bit array multiplier. A chain of four inverters is used to characterize the energy-delay product and the power consumption for activity factors of 25%, 50%, and 100%. In addition, the robustness of the logic families to noise and variability is evaluated by analyzing the noise margins of a chain of inverters and the threshold voltage variation of universal gates. The 4×4 array multiplier is used to characterize process, voltage, and temperature variation through corner analysis, and to characterize the statistical local and global variation through

Table 1
Comparison of the performance, area, and power consumption of an inverter chain operating at a 400 mV supply voltage.

	CMOS	CML	DCML	LDCML	DFCML
f_{max} with 4 stages (MHz)	63	70	115	100	70
Area $(\mu m)^2$	2.88	10.56	4.56	4.85	3.0576
Static power (nW)	0.54	4550	0.2	0.14	0.12862
Dynamic power (nW)	544.46	300	368.8	393.86	240.97
Total power (nW)	545	4850	369	394	241.1

Table 2
Comparison of the performance, area, and power consumption of an inverter chain operating at a 450 mV supply voltage.

	CMOS	CML	DCML	LDCML	DFCML
f_{max} with 4 stages (MHz)	143	157	170	158	161
Area $(\mu m)^2$	2.88	10.56	4.56	4.85	3.0576
Static power (nW)	0.65	11797	0.22	0.15	0.14
Dynamic power (nW)	1634.35	1243	1077.8	1155.85	727.56
Total power (nW)	1635	13040	1078	1156	727.7

Monte Carlo analysis of the propagation delay and total power consumption. The SPICE simulations are performed using Cadence Spectre on a 130 nm CMOS technology, where the near-V_t voltages of 400 mV and 450 mV are considered. For the 130 nm fabrication process, the threshold voltage of the NMOS and PMOS transistors is, respectively, 0.35 ± 0.05 V and -0.33 ± 0.05 V. The maximum operating frequency of the logic families is determined as the time required for the output node to reach the full voltage swing within 70% of the active high clock for the DCML, LDCML, and DFCML logic families or 70% of the signal pulse width for the CML and CMOS gates. In other words, the maximum allowed propagation delay is set to 70% of the evaluation phase, which is equivalent to 85% of the signal period for the CML/CMOS logic families, assuming a 50% duty cycle. At a near-V_t voltage of 400 mV, for an input signal with a period of 16.66 ns (60 MHz operating frequency), the output is determined such that a full voltage swing is obtained within 14.161 ns.

4.1. Characterization of the maximum operating frequency, power consumption, and area

Three types of circuit topologies are implemented to analyze the total area, power consumption, and maximum operating frequency of each developed logic family. The topologies include 1) a chain of four inverters, 2) a universal gate (AND, OR, NAND, and NOR), and 3) a 4×4 bit array multiplier.

4.1.1. Characterization of logic families using a chain of four inverters

The maximum operating frequency, power consumption (static, dynamic, and total), and area of a chain of four inverters implemented with the CMOS, CML, DCML, LDCML, and DFCML logic families at 400 mV and 450 mV are listed in Tables 1 and 2, respectively. Each logic family is designed for minimum area and full voltage swing at the output of the fourth stage.

At all supply voltages and among all logic families, DCML operates at the highest frequency and CMOS at the lowest, where the maximum operating frequency of a CMOS inverter chain at 400 mV and 450 mV is, respectively, 63 MHz and 143 MHz. Therefore, for a fair analysis and comparison of the power and robustness to noise and variation, the inverter chains implemented in all logic families are set to an operating frequency of 60 MHz at 400 mV and 140 MHz at 450 mV. Among all differential signal based logic families, DFCML occupies the smallest area, with an increase of 1.06× as compared to CMOS. Both LDCML and DFCML exhibit up to a 1.68× increase in area as compared to CMOS, while the inverter chain implemented with CML resulted in an increase in area of 3.7× that of CMOS. In addition, the results listed in Tables 1 and 2 indicate a significant change in the optimum performance-power point when the supply voltage is increased from 400 mV to 450 mV. The 50 mV increase in the supply voltage results in, on average, an f_{max} that improves by approximately 2× and a total power consumption that increases by roughly 2.5×.

For both near-V_t operating voltages, the inverter chain implemented with DFCML dissipates the least total power with a consumption of 0.45× that of a CMOS inverter chain while providing a maximum operating frequency 1.13× that of CMOS. In comparison, at both near-V_t voltages, the DCML inverter chain consumes a total power of 0.68× and improves the maximum operating frequency by at least 1.19× that of a CMOS inverter chain. For both supply voltages, the total power consumption is reduced to 0.08× with at least a 1.08× improvement in the maximum operating frequency when comparing DCML to CML. The comparison of power and performance, therefore, varies with a reduction of 50 mV in the near-V_t supply voltage, as a greater drop in the maximum operating frequency is observed for CML (0.45×) and CMOS (0.44×) circuits as compared to DCML (0.68×) and LDCML (0.63×) circuits, where the CMOS inverter chain operating at a supply voltage of 450 mV provides the baseline for comparison.

The transient behavior of a chain of four inverters is shown in Fig. 7. The LDCML family exhibits the maximum power consumption and area among the three DDSL families. Therefore, only the LDCML chain of inverters is evaluated through transient analysis and compared with both the CML and CMOS chain of inverters. An iso-area comparison is performed, where the area of the CML and CMOS chain of inverters are resized to match the area of the LDCML chain of inverters (4.85 μm^2). The SPICE simulation is performed on a chain of four inverters set to a supply voltage of 450 mV and a frequency of 140 MHz. The average power consumption per cycle of the CMOS, CML, and LDCML chain of inverters is, respectively, 1.408 μW, 7.3 μW, and 0.74 μW. Despite the same area, operating frequency, and supply voltage, the LDCML chain of inverters consumes significantly less average power.

4.1.2. Characterization of logic families using universal gates

A characterization of the maximum operating frequency and active area is performed for universal gates implemented using all logic families at a near-V_t voltage of 450 mV, with results shown in Fig. 8. The DCML universal gate exhibits a maximum operating frequency of 280 MHz, which is an improvement in the peak frequency of 1.83× and 1.56× that of, respectively, CMOS NAND/NOR gates and a CML uni-

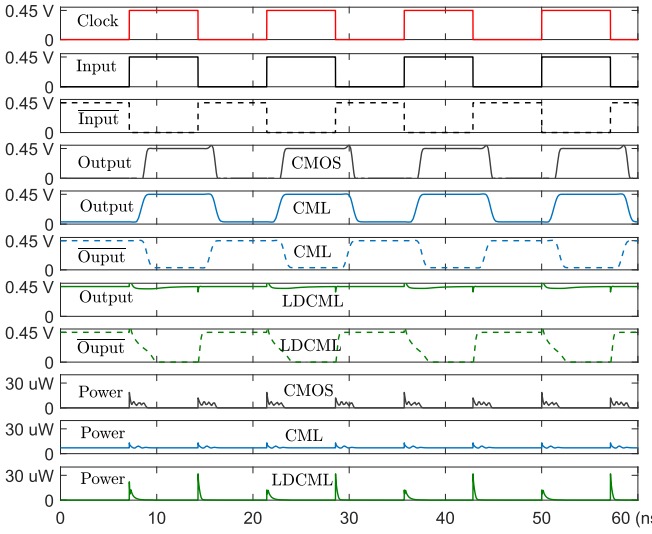


Fig. 7. Transient simulation for iso-area comparison of a CMOS, CML, and LDCML chain of four inverters operating at 450 mV and 140 MHz.

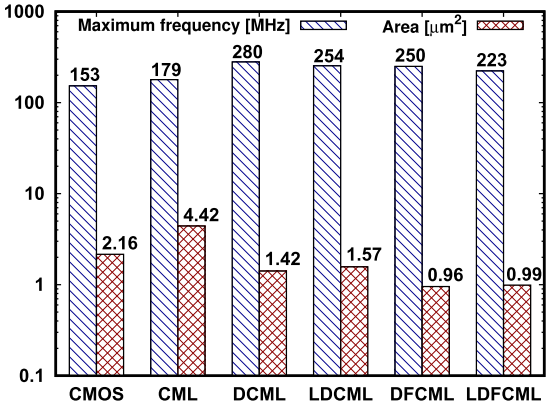


Fig. 8. Characterization of the maximum operating frequency and area of universal gates with a supply voltage of 450 mV. CMOS NAND/NOR gates were implemented for comparison.

versal gate. In addition, both DFCML and LDFCML exhibit at least a 1.63× improvement in the maximum operating frequency as compared to CMOS NANDs and NORs. Among all logic families, the DFCML universal gates occupy the smallest area, where the area of CMOS NAND/NOR and CML universal gates is, respectively, 2.26× and 4.63× greater than that of DFCML universal gates. The opposite behavior is observed for the inverter chain, where the CMOS implementation occupied the least area. Unlike standard CMOS circuits, the pull up network and voltage headroom are not significantly impacted when switching from an inverter to a NAND or NOR gate when using DFCML. As an example, the implementation of two-input DCML NAND and NOR gates, as compared to an inverter, require an additional series connected NMOS transistor in one of the two discharging paths (see Fig. 6 (a)), while the pull up network remains unchanged. In contrast, the CMOS NAND or NOR gate, as compared to an inverter, requires an additional transistor in both the pull up and pull-down network for each additional input.

The universal gates implemented using all logic families are characterized for static, dynamic, and total power consumption at a near-V_t voltage of 450 mV, with the results provided in Fig. 9. The static power of the CMOS NOR and CML universal gate is, respectively, 11× and 28.5× greater than that of a DCML universal gate. In addition, the use

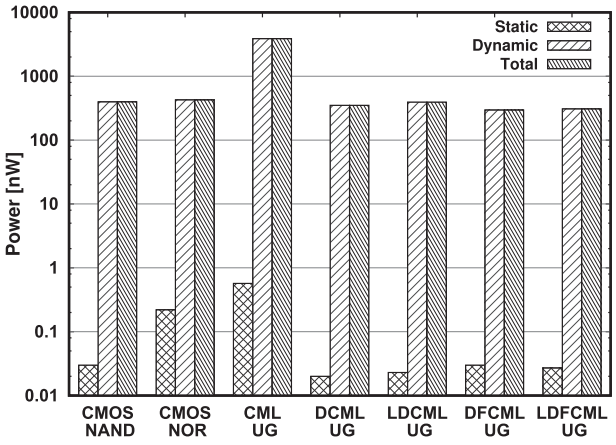


Fig. 9. Characterization of the power consumption of universal gates (UG) at a supply voltage of 450 mV.

of DCML and DFCML universal gates reduces the total power consumption to, respectively, 0.82× and 0.7× that of a CMOS NOR gate. The total power consumption of the CML universal gate is at least 9.8× greater than any of the DDSL universal gates. The analysis of the static, dynamic, and total power consumption of the universal gates implemented with all logic families indicates similar behavior as the four-stage inverter chain.

4.1.3. Characterization of logic families with a 4×4 bit array multiplier

The maximum operating frequency, total area, and total power consumption of a 4×4 bit array multiplier implemented in each logic family is characterized at a supply voltage of 450 mV. The results are normalized to the respective values of a CMOS multiplier and are shown in Fig. 10. The total area, maximum operating frequency, static power consumption, dynamic power consumption, and total power consumption of a 4×4 array multiplier implemented in CMOS are, respectively, 150.904 μm^2, 20 MHz, 0.01185 μW, 3.60315 μW, and 3.615 μW. Similar to the inverter chain and universal gates, multipliers implemented using DCML, LDCML, and DFCML exhibit improved performance as compared to CMOS and CML. The maximum operating frequency of the DDSL families is at least 1.4× and 1.12× greater as compared to, respectively, CMOS and CML multipliers. The total area of the DCML multipliers is 1.5× and 0.57× the area of, respectively, the CMOS and CML multipliers. The total power consumption of LDCML and DFCML multipliers, which is approximately equal, is 0.9× and 0.009× the total power consumption of, respectively, a CMOS and CML multiplier. However, a DCML multiplier consumes 1.48× the total power of a CMOS multiplier. The increase in the area and power consumption of a DCML multiplier is a result of the added buffers used to restore the full voltage swing of the signal at the output.

4.2. Characterization of static, dynamic, and total power consumption for different activity factors

A chain of four inverters is implemented in each logic family to analyze the effect of activity factor on the power consumption. For CMOS circuits, the dynamic power consumption is reduced with lower circuit activity. However, for DDSL, the dynamic power does not change with activity factor as the output terminals of a DDSL circuit are always charged and discharged during, respectively, the pre-charge and evaluate phases. The power consumption is, therefore, relatively constant regardless of input activity. CML circuits exhibit minor changes in the power consumption with a change in activity factor as the dominant component is the static power dissipation. The power consumption of each logic family for activity factors of 25%, 50%, and 100% and for a supply voltage of 400 mV is shown in Fig. 11. The total power consump-

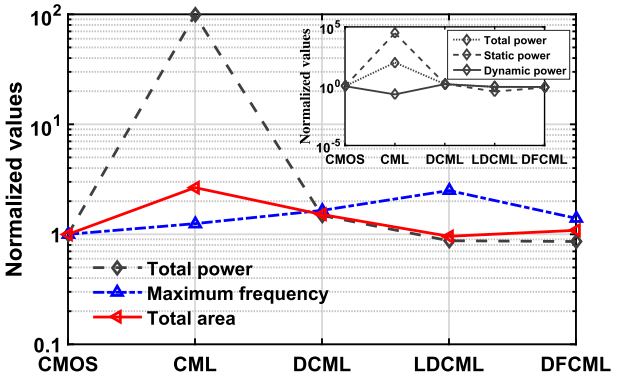


Fig. 10. Power, area, and maximum operating frequency of a 4×4 bit array multiplier implemented in all logic families.

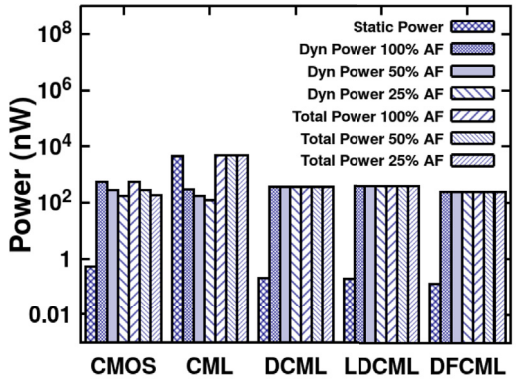


Fig. 11. Power consumption of a chain of four inverters implemented with all logic families for activity factors of 25%, 50%, and 100% and for a supply voltage of 400 mV.

tion (dynamic and static) is calculated as the average power per cycle over 60 cycles for each activity factor. For all logic families, the operating frequency of the inverter chain is set to 60 MHz. Among all logic families, the DCML, LDCML, and DFCML inverter chains consume the minimum static power, where the static power consumption of the three families is approximately 0.05% of the total power consumption. The majority of the total power consumed by CML is static since, regardless of input activity or switching events, there is a constant static current through the tail transistor. The majority of the total power consumption of the DDSL families, however, is dynamic as there is a periodic charging and discharging of the output nodes. The use of DDSL over CML results in additional power savings as the static current path through the tail transistor is no longer present.

4.3. Characterization of energy-delay product (EDP)

An analysis of the energy-delay product (EDP) for all logic families is performed using a four-stage inverter chain. The supply voltage is set to 450 mV and the operating frequency to 60 MHz. The two middle stages are considered when determining the EDP to more accurately represent the input and output capacitive loads and intrinsic delay of the inverters. The characterization of EDP for all logic families is provided through the results shown in Fig. 12, where all values are normalized to the EDP of a CMOS inverter chain (0.02×10^{-20} J·s). All DDSL families exhibit improved EDP as compared to both the CMOS and CML inverter chains. LDCML exhibited the minimum EDP, which is approximately 0.07× and 0.004× the EDP of, respectively, CMOS and CML.

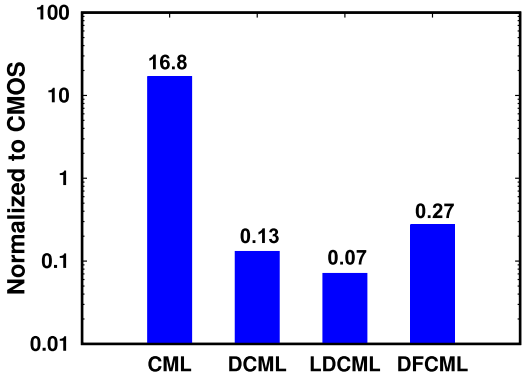


Fig. 12. Energy delay product of a chain of inverters operating at a supply voltage of 450 mV. All values are normalized to the EDP of a CMOS inverter chain (0.02×10^{-20} J·s).

4.4. Characterization of circuit robustness to noise

One of the key challenges of near-threshold computing (NTC) is a reduced robustness to external noise due to a scaled supply voltage. The robustness of the dynamic differential signaling logic (DDSL) families is, therefore, analyzed and compared with CML and CMOS logic circuits. The robustness is evaluated through 1) an analysis of the noise margin, where a novel method to identify the noise margins of differential logic circuits is introduced, and 2) an analysis of the sensitivity of the logic families to threshold voltage variation. The effect of process, voltage, and temperature (PVT) variations on the propagation delay and total power consumption is also analyzed. External sources of noise, including power supply noise and crosstalk due to inductive, capacitive, and conductive coupling, are considered through noise margin analysis. In addition, both global and local process variation and mismatch variation is characterized through Monte-Carlo simulation.

4.4.1. Analysis of noise margins

The analysis of the worst case variation of the noise margins is performed for a single inverter in all logic families at a supply voltage of 400 mV and with a set frequency of 60 MHz. For the CMOS inverter, a conventional voltage transfer curve (VTC) is analyzed [37]. Both CML and DDSL inverters are, however, evaluated by differential inputs and outputs. The inverter VTC curve, therefore, represents the input and output as the difference between, respectively, the two input and two output signals. The method of measuring noise margins for differential logic families is illustrated through Fig. 13, where the solid black line and the dotted blue line represent, respectively, the differential input and differential output. The noise margins are determined for values when the derivative of the differential output voltage is −1. For differential logic circuits, the noise margins are evaluated using (11), where x is the differential input voltage between In and $\overline{In}$, y is the differential output voltage between Out and $\overline{Out}$, and N is the value of x for which $|\frac{dy}{dx}|$ is equal to 1. The two points of the derivative curve that are equal to −1 and fall within the transition region of the VTC are ignored. The transition points A and B shown in Fig. 3 are determined for differential based logic families using the proposed technique.

$$NM = V_{dd} - N, \tag{11}$$

where,

N = the value of x for which $|\frac{dy}{dx}| = 1$, $x = V_{In} - V_{\overline{In}}$, and $y = V_{Out} - V_{\overline{Out}}$.

The VTCs of the differential logic families are shown in Fig. 14 for a supply voltage of 400 mV. The LDCML and DFCML inverters exhibit

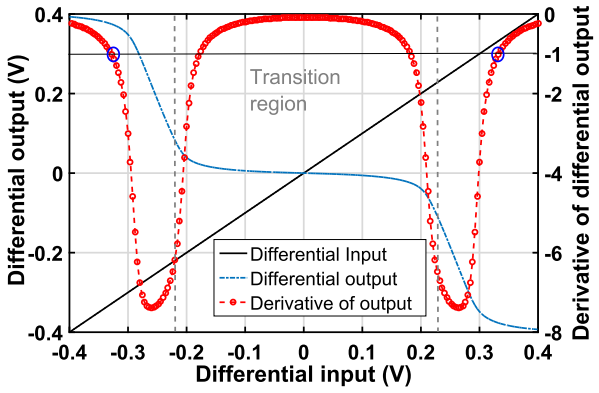


Fig. 13. VTC characterization to determine the noise margins of a DCML inverter at a supply voltage of 400 mV.

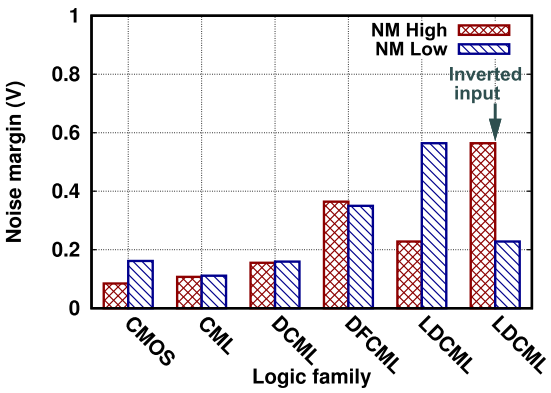


Fig. 15. Comparison of the noise margins of the logic families at a near-threshold voltage of 400 mV.

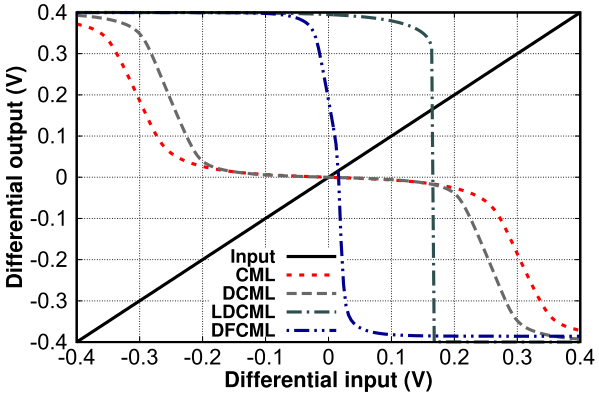


Fig. 14. VTC of all differential inverters at a 400 mV supply voltage.

a sharp transition from logic high to logic low. The CML and DCML inverters include an undefined region (logically indiscernible between logic high and logic low) for differential input signals between −0.2 V and 0.2 V, where the differential output remains close to 0 V. The result is a reduction in the noise margins of the CML and DCML circuits as compared to the LDCML and DFCML circuits. The noise margins of all logic families are shown in Fig. 15. The high noise margin (NM_H) is always a positive voltage while the low noise margin (NM_L) is always negative for the differential inverters. However, for ease of analysis and comparison, the absolute value of the NM_L is provided in Fig. 15 for all differential inverters.

$$V_{Tn} = V_{Tp} = V_T \tag{12}$$

$$k_R = \frac{k_n}{k_p} = 1 \tag{13}$$

$$k_n = \mu_n C_{ox}(\frac{W}{L})_n \tag{14}$$

$$k_p = \mu_p C_{ox}(\frac{W}{L})_p \tag{15}$$

The noise margins of the LDCML and DFCML inverters are larger than the DCML, CML, and CMOS inverters, where the DFCML inverter exhibits mean noise margins of 350 mV. The mean noise margin of the LDCML and DFCML inverters is at least 2.25× greater than the mean noise margin of a CMOS inverter. At near-V_t, the NM_H and NM_L of a LDCML inverter are, respectively, 228 mV and 564 mV when an initial differential voltage of 400 mV is applied at the input. Applying the negative differential input of −400 mV, results in a swap of the NM_H and NM_L to, respectively, 564 mV and 228 mV (inverted input in Fig. 15). The NM_H and NM_L of a CMOS inverter are, respectively, 161 mV and 90 mV. The symmetric VTC behavior of a CMOS inverter is not maintained at near-V_t to optimize the operating frequency of the gate, while minimizing the increase in area and power consumption. Equal noise margins are achieved when satisfying (12) and (13) for k_n and k_p given by, respectively, (14) and (15), where μ_n is the electron surface mobility, μ_p is the hole surface mobility, and W the width and L the length of the transistor [12,37]. The threshold voltages and, therefore, noise margins, also vary with changes in PVT and substrate bias. For a 130 nm technology, the variations in PVT and a non-zero substrate bias result in variations in the threshold voltage of up to 100 mV from the nominal value of 350 mV [15]. Disparate NMOS and PMOS threshold voltages and drive strengths, therefore, lead to differences in the values of the NM_H and NM_L.

Due to the PMOS keeper transistors, the input-output characteristics of LDCML circuits are sensitive to the polarity and magnitude of the initial input voltages, which results in disparate high and low noise margins. Inputs with equal applied voltages result in a similar voltage at the two output nodes unless one of the inputs changes with respect to the other. The VTC for a differential input voltage of 0 V when both input nodes are initially equal is shown in Fig. 16 as LDCML output 2. However, for the analysis of the noise margins, a non-zero initial differential input voltage is applied, corresponding to LDCML output 1 in Fig. 16, as equal voltages at the inputs results in the inverter not functioning as intended. The asymmetric behavior of the noise margins is not present when the size of the NMOS transistors is increased by 20×, which results in a symmetric response as shown by LDCML output 3 in Fig. 16. The large NMOS transistors sink current from the output node with a moderate gate voltage, even as the holding PMOS keeper is supplying additional charge. As a result, the NM_L and NM_H are equal regardless of the input polarities. However, the increased size of the NMOS transistors results in a larger capacitive load and, therefore, higher power consumption, while also negating the charge restoration at the output nodes provided by the PMOS keepers. In addition, the asymmetric behavior of the VTC only occurs when the differential input voltage is between −0.15 V and 0.15 V, which are voltages not within the permitted operating point of the circuit. The asymmetric behavior of the noise margins of the LDCML inverter, therefore, does not effect the circuit operation, while providing additional power savings and performance benefits as compared to the symmetric implementation. Depending on the application and specific circuit biasing conditions, the differential inputs are set to either enhance the NM_H or NM_L of a LDCML circuit.

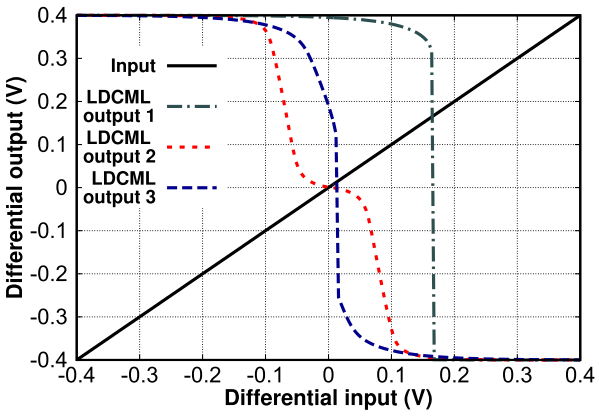


Fig. 16. VTC of a LDCML inverter with a supply voltage of 400 mV. An initial −400 mV differential input results in LDCML output 1, whereas an initial 0 V differential input results in LDCML output 2. A symmetric VTC is exhibited by LDCML output 3.

4.4.2. Characterization of logic families under threshold voltage variation

Near-threshold circuits suffer from inherent sensitivity to variation as a small change in the threshold voltage or supply voltage significantly impacts the optimum operating point. In addition, advanced technology nodes are more susceptible to the effects of process variation including fluctuations in the doping profile and the oxide thickness [12,37], which significantly impact the threshold voltage and, therefore, the performance and power consumption of the circuit. The threshold voltage is dependent on biasing conditions and on process parameters including silicon and oxide materials, physical dimensions, and doping concentrations [12,37]. The non-zero substrate bias threshold voltage V_T of a MOSFET is given by (16), and includes the zero substrate bias threshold voltage V_{T0} given by (17), where Φ_{GC} is the difference in the work function between the gate and channel, Q_{B0} is the charge density of the depletion region for a zero substrate bias, Q_{ox} is the charge density at the interface between the oxide and silicon, φ is the fermi potential, and γ is the substrate bias coefficient (body effect). The substrate bias coefficient given by (18) is dependent on the electron charge q, the doping concentration N_A, the dielectric constant of silicon ϵ_{si}, and the gate oxide capacitance per unit area C_{ox} [12,37].

$$V_T = V_{T0} + \gamma(\sqrt{|-2\varphi + V_{SB}|} + \sqrt{|2\varphi|}) \tag{16}$$

$$V_{T0} = \Phi_{GC} - 2\varphi - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{17}$$

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{\sqrt{C_{ox}}} \tag{18}$$

Changes in the threshold voltage due to PVT variation and/or substrate body bias modify the drive current of the transistors. For a given gate to source voltage V_{GS} and drain to source voltage V_{DS}, a positive source to body voltage V_{SB} for an NMOS transistor increases the width of the depletion layer and reduces the drive current. The maximum operating frequency of the transistor is, therefore, reduced. Variations in process parameters impact both V_T and V_{T0} as indicated through evaluation of (16) and (17), respectively. For example, a larger Q_{B0}/C_{ox} ratio or Q_{ox}/C_{ox} ratio results in a reduction in the zero bias threshold voltage V_{T0}. In this case, for a given V_{GS} and V_{DS}, the reduced V_{T0} results in an increase in the drive current of the transistors and, therefore, an increase in the maximum operating frequency. The variation in the threshold voltage is analyzed to determine the effect on the maximum operating frequency of the universal gates implemented in each logic family. The percentage change in the maximum operating frequency of all logic families for a ±10% variation in the nominal zero bias threshold voltage V_{T0} is shown in Fig. 17. The variation in V_{T0} resulted in up to an approximately 5% fluctuation in the non-zero substrate bias threshold voltage V_T. The analysis of threshold voltage variation is performed at a near-V_t voltage of 450 mV for all logic families, and the results are compared with CMOS and CML gates.

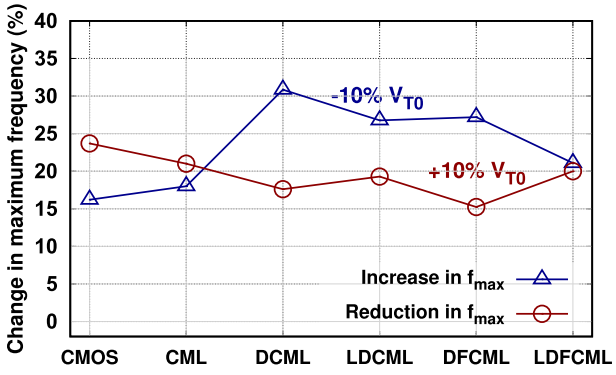


Fig. 17. Characterization of the maximum operating frequency f_{max} with ±10% variation in the threshold voltage of universal gates implemented in all logic families, where the maximum operating frequency at a supply voltage of 450 mV for all logic families is provided in Fig. 8.

The results indicate that there is a larger increase in the maximum operating frequency of the DDSL families as compared to CMOS and CML circuits with a reduction in the threshold voltage, as shown in Fig. 17. With a 10% reduction in V_{T0}, the DCML universal gate exhibits a 30.85% increase in the operating frequency, the largest amongst all logic families. In contrast, CMOS and CML circuits exhibit an increase in the maximum operating frequency of no more than 16.2% and 18%, respectively. Therefore, a 10% reduction in the threshold voltage results in up to a 1.7× increase in the frequency of a DDSL circuit as compared to a CML or CMOS circuit. With a 10% increase in V_{T0}, a DFCML circuit exhibits the smallest reduction in the operating frequency of 15.24% as compared to reductions of 23.7% and 21% for, respectively, CMOS and CML.

4.4.3. Characterization of logic families under process, voltage, and temperature variation

A characterization of process (*tt*, *ff*, and *ss*), voltage (from 0.35 V to 0.5 V), and temperature (from 27°C to 100°C) variations on a 4×4 bit array multiplier is performed. All logic families are analyzed at 20 MHz for iso-performance analysis as the CMOS multiplier exhibits a maximum operating frequency of 20 MHz at 450 mV. The change in the propagation delay and total power consumption of a 4×4 bit array multiplier due to variations in the process, voltage, and temperature are provided in, respectively, Tables 3, 4, and 5.

The propagation delay and total power consumption are characterized for the *tt*, *ff*, and *ss* corners as listed in Table 3 with the supply voltage set to 450 mV and the temperature to 27°C. All delay and power results are normalized to the delay and power of a CMOS multiplier operating in the *tt* corner, which are 14.3 ns and 3.615 μW, respectively. For the *ss* corner, the delay of a CMOS, CML, DCML, LDCML, and DFCML multiplier is, respectively, 1.6×, 0.9×, 0.3×, 0.4×, and 0.6× the delay of a CMOS multiplier operating in the *tt* corner. All DDSL multipliers exhibit greater variation among the three process corners (*tt*, *ss*, and *ff*) due to a larger number of transistors. For example, the delay of a CMOS inverter is affected by only two transistors, whereas the delay of a DDSL inverter is impacted by four transistors. The total power consumption of the CMOS, CML, DCML, LDCML, and DFCML multipliers operating at a frequency of 20 MHz in the *ff* corner is, respectively, 0.997×, 131×, 1.42×, 0.96×, and 0.94× that of the total power consumption of a CMOS multiplier operating in the *tt* corner.

Despite the lower maximum operating frequency of a DCML multiplier as compared to a LDCML multiplier, the 4×4 DCML multiplier incurs the shortest propagation delay. The shorter delay is due to: 1) As the number of logical stages implemented with DCML increases,

Table 3
Characterization of the propagation delay and total power consumption of a 4×4 bit array multiplier implemented in each logic family for three process corners at a supply voltage of 450 mV and temperature of 27°C. All delay and power results are normalized to, respectively, the delay and power of a CMOS multiplier operating in the *tt* corner and a temperature of 27°C.

Logic families	Propagation delay			Power consumption		
	tt	*ff*	*ss*	*tt*	*ff*	*ss*
CMOS	1	0.637	1.608	1	0.997	0.936
CML	0.589	0.387	0.897	98.5	131	74.5
DCML	0.157	0.082	0.318	1.479	1.423	1.615
LDCML	0.191	0.095	0.396	0.951	0.962	0.982
DFCML	0.206	0.085	0.634	0.952	0.943	1.0003

Table 4
Characterization of propagation delay and total power consumption of a 4×4 bit array multiplier implemented with all logic families for supply voltages between 0.35 V and 0.5 V. All delay and power results are normalized to, respectively, the delay (14.3 ns) and power consumption (3.615 μW) of a CMOS multiplier operating at a supply voltage of 0.45 V with the *tt* corner and a temperature of 27°C.

Logic families	Propagation delay				Power consumption			
	0.35 V	0.4 V	0.45 V	0.5 V	0.35 V	0.4 V	0.45 V	0.5 V
CMOS	5.406	2.189	1	0.531	0.428	0.674	1	1.265
CML	3.182	1.270	0.589	0.318	12.704	38.204	98.481	217
DCML	1.087	0.391	0.157	0.076	0.843	1.130	1.479	1.872
LDCML	1.770	0.585	0.191	0.081	0.477	0.701	0.952	1.225
DFCML	1.307	0.475	0.206	0.106	0.415	0.570	0.951	1.206

Table 5
Characterization of propagation delay and total power consumption of a 4×4 bit array multiplier implemented with all logic families at 27°C, 50°C, and 100°C, a supply voltage of 450 mV, and a process corner of *tt*. All delay and power results are normalized to, respectively, the delay (14.3 ns) and power consumption (3.615 μW) of a CMOS multiplier operating in the *tt* corner and at a temperature of 27°C.

Logic families	Propagation delay			Power consumption		
	27°C	50°C	100°C	27°C	50°C	100°C
CMOS	1	0.790	0.536	1	1.041	1.182
CML	0.589	0.477	0.338	98.5	122.8	178.9
DCML	0.157	0.120	0.080	1.479	1.559	1.824
LDCML	0.191	0.159	0.133	0.951	1.020	1.227
DFCML	0.206	0.163	0.114	0.952	1.021	1.201

the ability to provide full swing at the output node of the last stage decreases due to charge loss from the preceding logical stages during the evaluate phase, 2) although the propagation delay is calculated as the time difference between when an input and output signal change by 50%, full-swing at the output of DCML is not guaranteed, and 3) the condition set to determine the maximum operating frequency described in Section 4 requires the full swing within 70% of the active pulse width of the output. As a result, DCML and DFCML do not exhibit a higher f_{max} due to charge leakage at the output nodes.

The variation in the propagation delay and total power consumption of the multipliers implemented with CML, DCML, LDCML, and DFCML for supply voltages ranging from sub-V_t (0.35 V) to near-V_t (0.5 V) is listed in Table 4. The delay and power consumption of all multipliers operating at 27°C and in the *tt* process corner is determined and normalized to, respectively, the delay and power of a CMOS multiplier operating at a supply voltage of 0.45 V. The delay (power consumption) of a CMOS multiplier is 77.3 ns (1.55 μW), 31.3 ns (2.44 μW), 14.3 ns (3.615 μW), and 7.59 ns (4.58 μW) at a supply voltage of, respectively, 0.35 V, 0.4 V, 0.45 V, and 0.5 V. All DDSL multipliers exhibit up to a 3× increase in the normalized total power consumption as the supply voltage is scaled from a sub-V_t voltage of 0.35 V to a near-V_t voltage of 0.5 V, much less than the 17× increase seen for the CML multiplier. In addition, multipliers implemented with all logic families exhibit at least a 10× increase in the normalized propagation delay as the supply voltage is scaled from a near-V_t voltage of 0.5 V to a sub-V_t voltage of 0.35 V. The normalized propagation delay and total power consumption of the LDCML and DFCML multipliers are smaller as compared to a CMOS multiplier for all supply voltages between 0.35 V and 0.5 V.

The effect of temperature variation (from 27°C to 100°C) on the propagation delay and total power consumption of the logic families is analyzed, with results listed in Table 5. All delay and power results are normalized to, respectively, the delay and power consumption of a CMOS multiplier operating at 27°C, in the *tt* corner, and at 450 mV. The normalized delay and power varies less than 1.82× among all logic families when the temperature is increased from 27°C to 100°C. From all logic families, LDCML exhibits the greatest reduction in the normalized delay (0.7×) when the temperature increases to from 27°C to 100°C. The delay of the multiplier at a near-V_t voltage of 450 mV decreases with increasing temperature due to temperature effect inversion, while at super-V_t, higher temperatures result in larger delays [39–41]. All differential logic families exhibit higher variation in normalized power

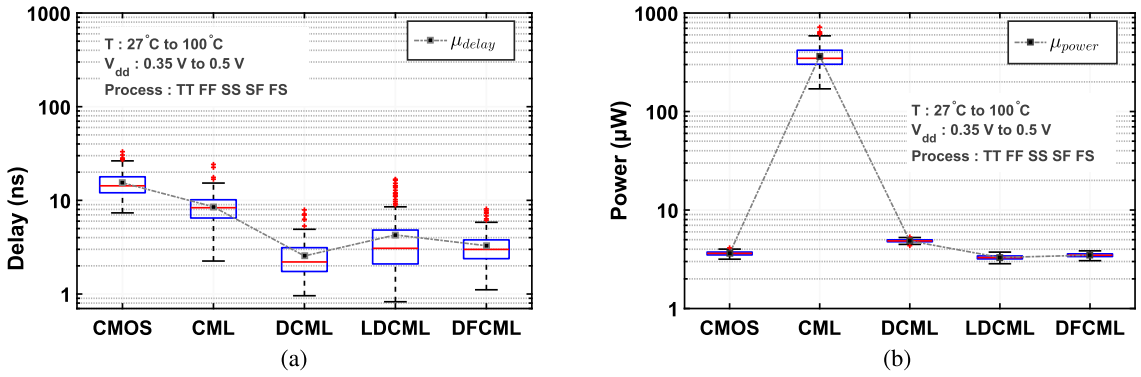


Fig. 18. Monte Carlo simulation with 200 runs of a 4×4 bit array multiplier to characterize a) delay and b) power consumption.

Table 6
Figures of merit at near-threshold voltage of 0.45 V (except NM_{avg}/V_{dd}, which is analyzed at 0.4 V). All results are normalized to CMOS logic operating at 1.2 V. Results for CML are from simulations by the authors. The topology of the CML universal gate described in [31] is implemented and characterized.

Logic Family	Reduction in Energy/Cycle	Reduction in f_{max}	Increase in NM_{avg}/V_{dd}	Area
CMOS [5,6]	≈10	≈14	Not given	Not given
CMOS	8.5	19.4	1.06	1
CML [31]	1.01	16.6	0.94	1.75
DCML	13.23	10.6	2.72	0.54
LDCML	10.9	11.7	3.42	0.63
DFCML	12.6	11.9	3.08	0.42

consumption as compared to a CMOS multiplier, where CML exhibits the greatest variation (1.82×) when the temperature is increased to 100°C from 27°C.

4.5. Analysis of local and global statistical variation

Process and mismatch are characterized using Monte-Carlo simulation with 200 runs to statistically analyze the variation in the propagation delay and total power consumption of the multipliers. The Latin-hypercube sampling method is applied, which allows for accurate process coverage with fewer runs [42]. Die-to-die and within-die variation are considered to characterize, respectively, global and local variation [43]. Five process corners (*tt*, *ff*, *ss*, *sf*, *fs*) and a temperature range of 27°C to 100°C are used for Monte-Carlo analysis of the logic families across supply voltages that fall between sub-V_t (0.35 V) and near-V_t (0.5 V).

The variation in delay and power is represented with a box-and-whisker plot as shown in, respectively, Fig. 18(a) and 18(b), to accurately analyze the population distribution. The mean value μ of both the delay and power is also provided in the figures for each logic family. The delay of all DDSL multipliers is less than that of a CMOS multiplier. The mean delay μ_{delay} of the CML, DCML, LDCML, and DFCML multipliers is, respectively, 0.55× (8.53 ns), 0.17× (2.55 ns), 0.28× (4.27 ns), and 0.21× (3.28 ns) the μ_{delay} of a CMOS multiplier (15.4 ns). The μ_{power} of the CML, DCML, LDCML, and DFCML multipliers is, respectively, 100× (365 μW), 1.34× (4.86 μW), 0.91× (3.30 μW), and 0.96× (3.48 μW) the μ_{power} of a CMOS multiplier (3.62 μW). In addition, the μ_{power} (μ_{delay}) of the DCML, LDCML, and DFCML multipliers is, respectively, 0.013× (0.3×), 0.009× (0.5×), and 0.009× (0.4×) the μ_{power} (μ_{delay}) of a CML multiplier. Therefore, both the delay and total power consumption is reduced with LDCML and DFCML multipliers as compared to CMOS and CML multipliers.

4.6. Comparison between near- and super-V_t operation

A comparison between circuits operating at a near-V_t voltage and at a super-V_t voltage is provided through results listed in Table 6, which includes data from prior research in NTC [5,6,31]. As the supply voltage is scaled from 1.2 V to 0.45 V, the reduction in energy/cycle, the reduction in f_{max}, the change in NM_{avg}/V_{dd}, and the change in area are characterized using universal gates. In addition, the effects of voltage scaling (1.2 V to 0.4 V) on the noise margins is analyzed using a chain of inverters. For CMOS logic, the scaling of the supply voltage from 1.2 V to 0.45 V reduces the energy/cycle by 8.5× at a cost of a 19.4× reduction in f_{max}, while prior research reported that scaling from super-V_t to near-V_t reduces the energy/cycle by approximately 10× and reduces the f_{max} by approximately 14× [5,6]. Therefore, the DCML, LDCML, and DFCML circuits consume less energy/cycle with a smaller reduction in f_{max}, which indicates that dynamic current mode logic families are more suitable for near-V_t operation over CML and CMOS logic families. In addition, the NM_{avg}/V_{dd} remains unchanged for CMOS when the supply voltage is scaled from 1.2 V to 0.4 V, while dynamic current mode logic families exhibit at least a 2.72× increase in NM_{avg}/V_{dd}.

4.7. Summary of results

Simulated results are summarized in Table 7 for a supply voltage of 450 mV, where an inverter chain, universal gates, multi-level logical functions, and a 4×4 bit array multiplier are used to characterize the DDSL families for area, power, operating frequency, noise margin, and EDP. The characterized values listed for of all logic families are normalized to the respective results of the CMOS equivalent gate. The dynamic differential signaling logic (DDSL) families are superior to CMOS and CML in total power consumption, maximum operating frequency, noise margin, EDP, and propagation delay. The DCML and DFCML families provide benefit for circuits with a fewer number of stages. However, LDCML is beneficial for any circuit size including a 4×4 bit array multiplier, as the total power, area, and maximum operating frequency are improved. The area of the LDCML chain of inverters is larger than an inverter chain implemented with CMOS, however, the opposite is observed for more complex logical functions including universal gates and a 4×4 bit array multiplier, where the CMOS implementation requires greater area. The improvement in total power con-

Table 7
Summary of results for all logic families normalized to CMOS for a supply voltage of 450 mV.

		CMOS (Baseline)	CML	DCML	LDCML	DFCML
Chain of inverters	Total power (at 60 MHz)	1 (1.635 μW)	8	0.66	0.7	0.45
	Maximum operating frequency	1 (143 MHz)	1.09	1.19	1.15	1.13
	Total area	1 (2.88 μm^2)	3.7	1.58	1.68	1.06
	Noise margin	1 (123 mV)	0.89	1.28	3.22	2.9
	EDP	1 (0.02×10^{-20} J·s)	16.84	0.13	0.071	0.27
Universal gates	Total power (at 140 MHz)	1 (0.427 μW)	9.07	0.82	0.92	0.7
	Maximum operating frequency	1 (153 MHz)	1.17	1.83	1.66	1.63
	Total area	1 (2.16 μm^2)	2.05	0.66	0.73	0.44
4×4 array multiplier	Total power (at 20 MHz)	1 (3.62 μW)	98	1.48	0.95	0.95
	Maximum operating frequency	1 (20 MHz)	1.25	1.65	2.5	1.4
	Total area	1 (151 μm^2)	2.7	1.5	0.96	1.09
	Propagation delay	1 (14.3 ns)	0.59	0.16	0.19	0.21

sumption and maximum operating frequency is, therefore, scalable to larger circuit blocks when DDSL families are used.

5. Conclusions

Three DDSL families are proposed and evaluated for near-threshold computing that are compared with CML and CMOS equivalent circuits. The comparison is performed through analysis of power consumption, propagation delay, maximum operating frequency, noise margins, and variations in threshold voltage, process parameters, supply voltage, and temperature using a chain of four inverters, universal gates, multi-level logical functions, and a 4×4 bit array multiplier. The LDCML and DFCML multipliers reduce the total power consumption to 0.96× and 0.009× that of, respectively, CMOS and CML multipliers, while improving the performance by 1.4× and 1.12×. At a supply voltage of 450 mV and operating frequency of 60 MHz, the EDP of the DDSL circuits is up to 0.27× and 0.016× the EDP of, respectively, CMOS and CML circuits. The mean noise margins of DFCML and LDCML are improved by at least 2.5× or more as compared to the mean noise margins of the CMOS circuits. In addition, the DDSL gates exhibit a minimum reduction in the maximum operating frequency when the threshold voltage is increased by 10%. The DDSL circuits also provide a reduction in the static power consumption and the potential to increase the number of stages at near-V_t supply voltages. The proposed DDSL families are, therefore, well suited for robust ultra-low power applications with moderate to low performance requirements as the DDSL families exhibit a higher operating frequency and robustness to noise at near-V_t voltages than either CMOS or CML.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mejo.2020.104801.

References

[1] M. Abdelfattah, M. Swilam, B. Dupaix, S. Smith, A. Fayed, W. Khalil, An on-chip resonant-gate-drive switched-capacitor converter for near-threshold computing achieving 70.2% efficiency at 0.92 A/mm^2 current density and 0.4 V output, Proceedings of the IEEE International Solid-State Circuits Conference, February 2018, pp. 438–440.

[2] S. Kiamehr, M. Ebrahimi, M.S. Golanbari, M.B. Tahoori, Temperature-aware dynamic voltage scaling to improve energy efficiency of near-threshold computing, IEEE Transactions on Very Large Scale Integration Systems, 25 (No. 7) (July 2017) 2017–2026.

[3] Y. Gu, D. Yan, V. Verma, M.R. Stan, X. Zhang, SRAM based opportunistic energy efficiency improvement in dual-supply near-threshold processors, Proceedings of the IEEE/ACM Design Automation Conference, June 2018, pp. 1–6.

[4] N. Pinckney, L. Shifren, B. Cline, S. Sinha, S. Jeloka, R.G. Dreslinski, T. Mudge, D. Sylvester, D. Blaauw, Near-threshold computing in FinFET technologies: opportunities for improved voltage scalability, Proceedings of the IEEE/ACM Design Automation Conference, June 2016, pp. 76: 1–6.

[5] H. Kaul, M. Anders, S. Hsu, A. Agarwal, R. Krishnamurthy, S. Borkar, Near-threshold voltage (NTV) design: opportunities and challenges, Proceedings of the IEEE/ACM Design Automation Conference, June 2012, pp. 1153–1158.

[6] R.G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, T. Mudge, "Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits, Proceedings of the IEEE, 98 (No. 2) (January 2010) 253–266.

[7] D. Marković, C.C. Wang, L.P. Alarcon, T. Liu, J.M. Rabaey, Ultralow-power design in near-threshold region, Proceedings of the IEEE, 98 (No. 2) (February 2010) 237–252.

[8] M.S. Hossain, I. Savidis, Reusing leakage current for improved energy efficiency of multi-voltage systems, IEEE International Symposium on Circuits and Systems, (May 2019) 1–5.

[9] A.P. Chandrakasan, S. Sheng, R.W. Brodersen, Low-power CMOS digital design, IEEE Journal of Solid State Circuits, 27 (No. 4) (April 1992) 473–484.

[10] R.G. Dreslinkski, B. Zhai, T. Mudge, D. Blaauw, D. Sylvester, An energy efficient parallel architecture using near threshold operation, Proceedings of the IEEE International Conference on Parallel Architecture and Compilation Techniques, September 2007, pp. 175–188.

[11] B. Zhai, R.G. Dreslinski, D. Blaauw, T. Mudge, D. Sylvester, Energy efficient near-threshold chip multi-processing, Proceedings of the IEEE/ACM International Symposium on Low Power Electronics and Design, August 2007, pp. 32–37.

[12] J.M. Rabaey, A.P. Chandrakasan, B. Nikolic, Digital Integrated Circuits, second ed., Prentice Hall Englewood Cliffs, 2002.

[13] R.M. Swanson, J.D. Meindl, Ion-implanted complementary MOS transistors in low-voltage circuits, IEEE Journal of Solid State Circuits, 7 (No. 2) (April 1972) 146–153.

[14] B.H. Calhoun, A. Chandrakasan, Characterizing and modeling minimum energy operation for subthreshold circuits, Proceedings of the IEEE/ACM International Symposium on Low Power Electronics and Design, August 2004, pp. 90–95.

[15] N.S. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, V. Narayanan, "Leakage current: Moore's law meets static power, Computer 36 (No. 12) (December 2003) 68–75.

[16] J. Kwong, A.P. Chandrakasan, Variation-driven device sizing for minimum energy sub-threshold circuits, Proceedings of the International Symposium on Low Power Electronics and Design, October 2006, pp. 8–13.

[17] V.M.V. Santen, J. Martin-Martinez, H. Amrouch, M.M. Nafria, J. Henkel, Reliability in super-and near-threshold computing: a unified model of RTN, BTI, and PV, IEEE Transactions on Circuits and Systems I: Regular Paper, 65 (No. 1) (January 2018) 293–306.

[18] Z. Wang, S. Yin, F. Tu, L. Liu, S. Wei, An Energy efficient JPEG encoder with neural network based approximation and near-threshold computing, Proceedings of the IEEE International Symposium on Circuits and Systems, May 2018, pp. 1–5.

[19] X. Zhang, T. Tong, S. Kanev, S.K. Lee, G. Wei, D. Brooks, Characterizing and evaluating voltage noise in multi-core near-threshold processors, Proceedings of the International Symposium on Low Power Electronics and Design, September 2013, pp. 82–87.

[20] A. Gebregiorgis, S. Kiamehr, F. Oboril, R. Bishnoi, M.B. Tahoori, A cross-layer analysis of soft error, aging and process variation in near threshold computing, Proceedings of the Design, Automation and Test in Europe Conference and Exhibition, March 2016, pp. 205–210.

[21] R. Taco, I. Levi, M. Lanuzza, A. Fish, An 88-fJ/40-MHz [0.4 V]–0.61-pJ/1-GHz [0.9 V] dual-mode logic 8x8 bit multiplier accumulator with a self-adjustment mechanism in 28-nm FD-SOI, IEEE Journal of Solid State Circuits, 54 (No. 2) (2019) 560–568.

[22] J.W. Davis, L.G. Heller, W.R. Griffin, N.G. Thoma, Cascode voltage switch logic: a differential CMOS logic family, Proceedings of the IEEE International Solid-State Circuits Conference, February 1984, pp. 16–17.

[23] M.W. Allam, M. Elmasry, Dynamic current mode logic (DyCML): a new low-power high-performance logic style, IEEE Journal of Solid State Circuits, 36 (3) (October 2001) 550–558.
[24] A. Shapiro, E.G. Friedman, MOS current mode logic near threshold circuits, Journal of Low Power Electronics and Applications, 4 (No. 2) (June 2014) 138–152.
[25] M.S. Hossain, I. Savidis, Robust near-threshold inverter with improved performance for ultra-low power applications, Proceedings of the IEEE International Symposium on Circuits and Systems, May 2016, pp. 738–741.
[26] M.S. Hossain, I. Savidis, Dynamic current mode inverter for ultra-low power near-threshold computing, Proceedings of the Government Microcircuit Applications and Critical Technology Conference,, March 2016, pp. 409–412.
[27] L. Heller, W. Griffin, J. Davis, N. Thoma, Cascode voltage switch logic: a differential CMOS logic family, Proceedings of the IEEE International Solid-State Circuits Conference, February 1984, pp. 16–17.
[28] P. Ng, P.T. Balsara, D. Steiss, Performance of CMOS differential circuits, IEEE Journals of Solid State Circuits, 31 (No. 6) (June 1996) 841–846.
[29] J.M. Musicer, J. Rabaey, MOS current mode logic for low Power, low noise CORDIC computation in mixed-signal environments, Proceedings of the International Symposium on Low Power Electronics and Design, July 2000, pp. 102–107.
[30] M. Yamashina, H. Yamada, An MOS current mode logic (MCML) circuit for low-power sub-GHz processors, Transactions on Electronics, 75 (No. 10) (October 1992) 1181–1187.
[31] Y. Bai, Y. Song, M.N. Bojnordi, A. Shapiro, E. Ipek, E.G. Friedman, Architecting a MOS current mode logic (MCML) processor for fast, low noise and energy-efficient computing in the near-threshold regime, Proceedings of the IEEE International Conference on Computer Design, December 2015, pp. 527–534.
[32] T. Liu, L.P. Alarcón, M.D. Pierson, J.M. Rabaey, Asynchronous computing in sense amplifier-based pass transistor logic, IEEE Transactions on Very Large Scale Integration Systems, 17 (No. 7) (July 2009) 883–892.
[33] L. Amarú, P. Gaillardon, J. Zhang, G.D. Micheli, Power-gated differential logic style based on double-gate controllable-polarity transistors, IEEE Transactions on Circuits and Systems II: Express Brief, 60 (No. 10) (August 2013) 672–676.
[34] M.T. Moreira, M.E. Arendt, F.G. Moraes, N.L.V. Calazans, Static differential NCL gates: toward low power, IEEE Transactions Circuits and Systems II: Express Brief, 62 (No. 6) (June 2015) 563–567.
[35] Z. Chen, M. Lin, Y. Zheng, Z. Wei, S. Huang, S. Zou, Single-event transient characterization of a radiation-tolerant charge-pump phase-locked loop fabricated in 130 nm PD-SOI technology, IEEE Transactions on Nuclear Science, 63 (No. 4) (July 2016) 2402–2408.
[36] A. Bellaouar, "Current mode logic gates for low-voltage high speed applications," July 24 2001, US Patent 6,265,898.
[37] E. Salman, E.G. Friedman, High Performance Integrated Circuit Design, McGraw Hill Professional, 2012.
[38] G. Palumbo, M. Pennisi, M. Alioto, A simple circuit approach to reduce delay variations in domino logic gates, IEEE Transactions on Circuits and Systems I: Regular Paper, 59 (No. 10) (October 2012) 2292–2300.
[39] W. Lee, Y. Wang, T. Cui, S. Nazarian, M. Pedram, Dynamic thermal management for FinFET-based circuits exploiting the temperature effect inversion phenomenon, Proceedings of the International Symposium on Low Power Electronics and Design, August 2014, pp. 105–110.
[40] W. Lee, K. Han, Y. Wang, T. Cui, S. Nazarian, M. Pedram, TEI-Power: temperature effect inversion–aware dynamic thermal management, ACM Transactions on Design Automation of Electronic Systems, 22 (No. 3) (April 2017) 51.
[41] K. Han, J. Lee, J. Lee, W. Lee, M. Pedram, TEI-NoC: optimizing ultralow power NoCs exploiting the temperature effect inversion, IEEE Transactions on Computer-Aided Design Integrated Circuits and Systems, 37 (No. 2) (February 2018) 458–471.
[42] A.A. Mutlu, M. Rahman, Statistical methods for the estimation of process variation effects on circuit operation, IEEE Transactions on Electronics Packaging Manufacturing, 28 (No. 4) (October 2005) 364–375.
[43] K.A. Bowman, A.R. Alameldeen, S.T. Srinivasan, C.B. Wilkerson, Impact of die-to-die and within-die parameter variations on the throughput distribution of multi-core processors, Proceedings of the IEEE International Symposium on Low Power Electronics and Design, August 2007, pp. 50–55.