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Electrical modeling and characterization of through-silicon vias (TSVs) for 3-D integrated circuits

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ABSTRACT

The integration of chips in the third dimension has been explored to address various physical and system level limitations currently undermining chip performance. In this paper, we present a comprehensive analysis of the electrical properties of through silicon vias and microconnects with an emphasis on single via characteristics as well as inter-TSV capacitive and inductive coupling in the presence of either a neighboring ground tap or a grounded substrate back plane. We also analyze the impact of technology scaling on TSV electrical parasitics, and investigate the power and delay trend in 3-D interstratum IO drivers with those of global wire in 2-D circuits over various technology nodes. We estimate the global wire length necessary to produce an equivalent 3-D IO delay, a metric useful in early stage design tools for 3D floorplanning that considers the electrical characteristics of 3D connections with TSVs and microconnects.

1. Introduction

The continued miniaturization of microelectronics is becoming a challenge from both the technological and financial perspectives. Three-dimensional (3D) integration technology offers significant promise of improved performance and form factor without having to necessarily introduce finer devices. 3-D technology relies on electrical interconnection directly between multiple strata that are stacked on top of one another, thereby offering significantly reduced interconnection length as compared with equivalent 2-D systems like SoC. This wire length reduction translates into much improved interconnection delay and power. This, in addition to improved form factor and the integration of heterogeneous technologies, is among the most promising benefits of 3-D integration technology.

The realization of 3-D integrated circuits relies on novel process technologies. Metal-filled through-silicon vias (TSVs) provide electrical interconnection between two neighboring dice when the dice are bonded back-to-face or back-to-back, where back refers to the silicon substrate side and face refers to the metal interconnect side. At the bonded interface, metallic microconnect pads from two different strata are bonded to each other, offering the capability to transmit electrical signals with very small wire length. This bonding can be done either between two wafers, between a wafer and die or between two die. In addition, wafer or die thinning is also a critical process technology for realizing 3-D integrated circuits.

Much of the recent work on 3-D technology has focused on the development of process technologies required for manufacturing 3-D circuits [1–3]. Technologies such as wafer thinning, wafer-to-wafer and die-to-wafer bonding, and etching and filling of high-aspect-ratio vias in silicon have been developed. With the absence of design tools capable of understanding new design paradigms and performing design optimization in 3D ICs, there is also much need for understanding new design challenges and opportunities in 3D ICs. The possibility of die and mask-reuse in 3D ICs has been explored [4]. Design of multicore processors and core-on-logic systems using 3D ICs has been presented [5]. While device-level redesign of processors appears to be an unattractive option, there is certainly much interest in block-level partitioning and implementation in multiple strata. Thermal management concerns in 3D ICs have also been addressed [6], including the important issue of thermal–electrical optimization and co-design [7]. While on one hand, 3D technology has led to a rethinking of design paradigms, it is also important to electrically characterize

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through-silicon via (TSV) and microconnects, since these elements are unique to 3D technology, and not much prior knowledge of their electrical performance exists. Not only will such a study lead to an understanding of electrical parasitics introduced by these 3D interconnection elements, it will also enable system-level design of circuits that use TSVs and microconnects for interconnection. Further, it is important to develop compact electrical models of TSVs and micropads in order to understand the effect of technology scaling, particularly the effect of reduction of TSV radius and height on the electrical parasitics. The parasitic effects between multiple TSVs are also of significant practical importance.

Only limited work has been reported on the electrical performance of both through-silicon vias (TSVs) and microconnects (a microconnect is the metallic bonded portion comprised of copper or copper tin alloy) that provide interstratum connections [8–11]. A few authors have reported analytical expressions for resistance, capacitance, and inductance of a TSV [11,12]. The electrical characteristics of an array of TSVs have also been studied [13,14]. The sidewall dielectric thickness has been recognized as a critical parameter in determining TSV capacitance. While the separate determination of *R*, *L*, and *C* parameters is certainly more desirable, some work on S-parameter extraction for TSVs has also been reported [9].

In addition to the electrical performance of TSVs, the thermal and mechanical characteristics of TSVs is also important for system-level characterization of practical applications. Electrical, thermal and mechanical performance of TSVs are in fact closely coupled to each other [7]. Passage of electrical current through the TSV results in Joule heating and hence temperature rise. This places constraints on the TSV aspect ratio, since a thinner, longer TSV has a higher thermal resistance, and hence a higher temperature rise. Another consideration in the thermal performance of the TSV is the barrier layer, whose material is typically thermally insulating and thus, depending on the barrier layer thickness, may lead to significant temperature rise. The temperature rise in TSVs also leads to mechanical stress generation [15] due to an unequal thermal expansion coefficient between silicon and the TSV filler material. Further, this mechanical stress generation influences the electrical design since mechanical stress is known to influence transistor performance which may lead to design rules prohibiting circuit placement too close to TSVs.

This paper focuses on the electrical modeling and characterization of a TSV and microconnect with an emphasis on single via characteristics as well as inter-TSV capacitive and inductive coupling in the presence of either a neighboring ground tap or grounded substrate back plane. The single-TSV and TSV-to-TSV characterization presented in this work are expected to be useful for system-level simulations comprising a large number of TSVs. A full system-level simulation of hundreds or thousands of TSVs is unlikely to account for the geometrical features of each and every TSV, and will instead treat each TSV as an *RLC* equivalent. In order to do so, the *RLC* characteristics obtained in our work is the first step towards enabling system-level simulations.

We show that electrical characteristics significantly depend on neighboring structures, such as a ground tap and grounded substrate back plane, a phenomenon than can be exploited in circuit layout for desired electrical characteristics. Moreover, simulated electrical parasitics vary from the ideal analytical models when different operating conditions and neighboring structures are considered. We also analyze the impact of technology scaling on TSV electrical parastitics, and investigate the power and delay trend in 3-D interstratum IO drivers with those of global wire in 2-D circuits over various technology nodes. We estimate the global wire length necessary to produce an equivalent 3-D IO delay, a metric useful in early stage design tools for 3D floorplanning that considers the electrical characteristics of 3D connections with TSVs and microconnects.

The rest of the paper is organized as follows: Section 2 discusses the technology scaling trend of TSVs. The *R*, *L*, and *C* characterizations of TSVs for a range of various parameters are presented in Section 3. Section 4 analyzes the power consumption and time delay characteristics of interstratum signal transmission through a TSV and microconnect at various technology nodes. Results indicate that 3-D integration compares very favorably against global wire signal transmission. Drawn conclusions are presented in Section 5.

2. Through-Si via analytical model and technology scaling trend

As TSVs occupy space that would otherwise be available for active devices on the Si substrate, a reduction of the TSV footprint is necessary to minimize the Si area trade-off with technology scaling. Therefore, an analysis of the impact TSV scaling has on electrical parasitics is required. Neglecting end effects, for a cylindrical metal-filled TSV of height h, radius r_{via}, and dielectric (SiO_2) thickness t, we can employ the following equations to compute R and C:

$$R = \frac{\rho_m h}{\pi {r_{via}}^2} \tag{1}$$

$$C = \frac{2\pi\varepsilon_r\varepsilon_o h}{\ln((r_{via}+t)/r_{via})} \tag{2}$$

where ρ_m is the resistivity of the metal filling in the TSV, and ε_r and ε_o are the relative permittivities of SiO_2 and empty space, respectively. Note that r_{via} is the radius of the metal-filled region of the TSV. The overall TSV dimensions are limited by strata thinning and thin strata handling process capability. A practical TSV aspect ratio of 10:1 or lower is used as this is within current process capability [16]. For example, a substrate thinned down to 50 μm would limit a through-Si via footprint to 5 μm × 5 μm or larger. The substrate thickness, or equivalently the height of the TSV, needs to be reduced to scale down the TSV footprint. Further complications between the aspect ratio and TSV size interaction shown in our earlier study [11], indicate that the sidewall dielectric thickness needs to be quite high, such as 1 μm in a 5 μm × 5 μm TSV, in order to reduce parasitic capacitance. Therefore, the ratio of sidewall dielectric thickness and TSV radius

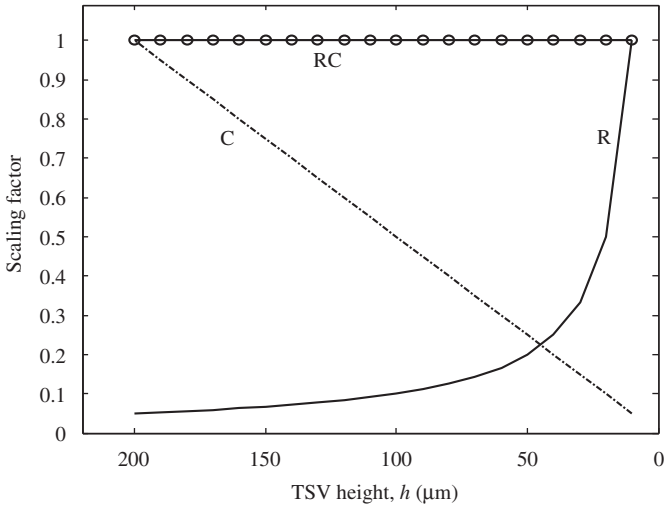

Fig. 1. Parasitic resistance and capacitance scaling trend of a TSV.

needs to be controlled to minimize parasitic capacitance while scaling down the TSV footprint.

Assuming a constant TSV aspect ratio and constant ratio of r_{via} and t in Eq. (2), we investigated the impact of TSV height (h) or equivalently the effect of substrate thinning. In this case, both the TSV radius r_{via} and sidewall thickness t scale linearly with via height. As illustrated in Fig. 1, the resulting R and C parameters scale inversely with respect to each other while the RC product remains unchanged (ignoring current crowding or scattering effects at the very small dimensions) with substrate thinning. Thus, a smaller TSV footprint in a thinner substrate would allow higher densities of interstratum connections while the RC product in the first order remains unchanged as technology nodes continue to scale.

3. Electrical characterization of through-Si vias

The analytical model for resistance and capacitance of a TSV presented in the previous section was extended to study more complicated cases, and to compute the inductance of TSVs. While through-Si vias for 3-D SOI technologies with a footprint of 1.75 μm × 1.75 μm and a length of 10 μm were shown to have a capacitance of 1–2 fF, 150–180 m Ω of resistance and 5–8 pH of inductance [17], results presented in this section pertain to bulk CMOS technology. Ansoft's Quick 3D (Q3D) toolset [18] was used to generate geometrical models of TSV-microconnects. A schematic of the geometry is shown in Fig. 2. A single via as well as a two-via case were investigated. In the single via case, the electrical characteristics of the 3-D via for various geometrical parameters were explored. For the two via case, the coupling capacitance and mutual inductance were investigated.

4. Single TSV characterization

The first electrical parameter characterized with Q3D was the capacitance of a single via. The capacitance was simulated with various lengths, widths and dielectric thicknesses for three cases: (a) assuming Si behaves like a fully conductive metal, (b) using Eq. (2) to solve for the capacitance analytically and (c) using a 1 μm thick ground plane on the backside of the semiconductor Si substrate. Results from the simulation are included in Fig. 3. Results for the various widths are not included as it produced similar results to the increasing length. Changes in width and length produced the same trends in capacitance. The capacitance increased from 35 to 55 fF linearly as the width was changed from 10 to 25 μm. The capacitance extracted from Q3D when silicon is considered a metal or the TSV is fully shielded agreed well with the value predicted by Eq. (2). Therefore, Eq. (2) produces the worst case capacitance for a TSV. When considering Si as a material with a conductivity of 10 S/m and a permittivity of 11.7ε_o

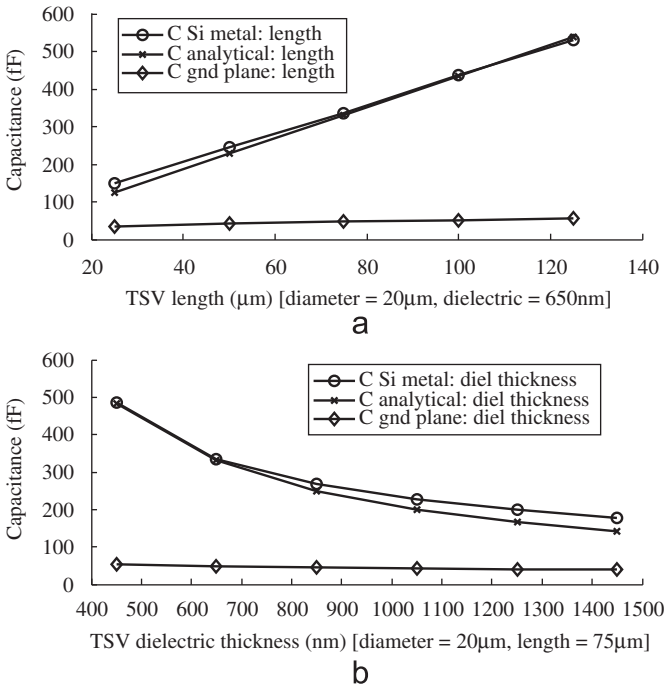

Fig. 3. Capacitance of a single 3-D for various lengths and dielectric thicknesses.

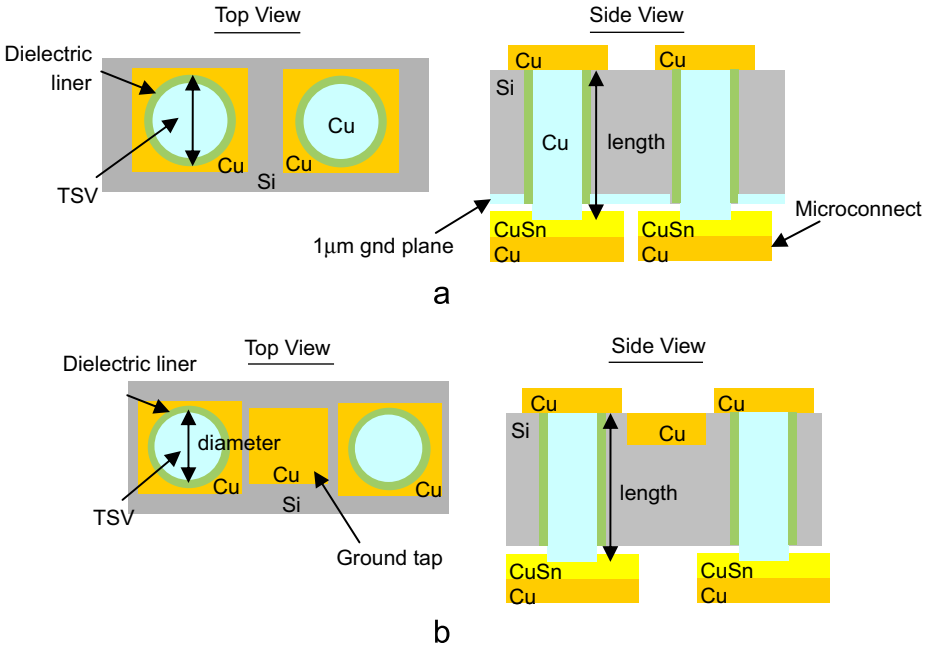

Fig. 2. Top and side view of the two copper 3-D vias. (a) a ground plane present, and (b) a ground tap replacing the ground plane.

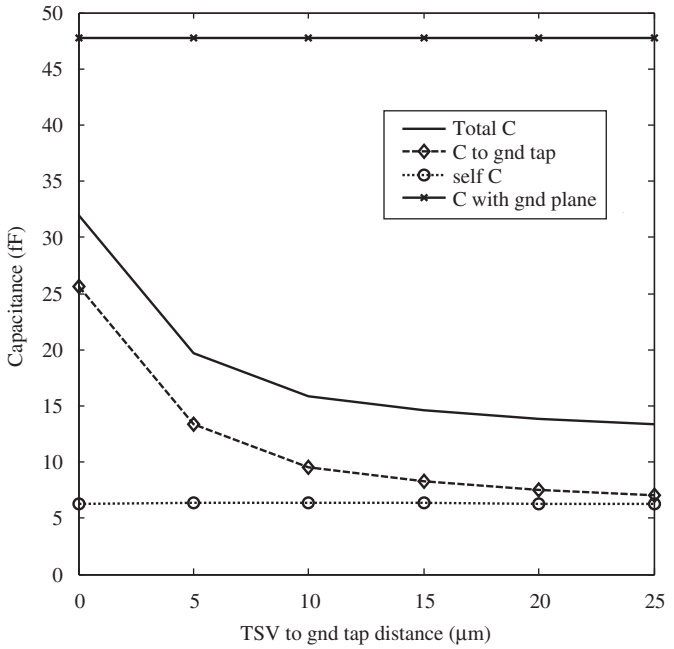

Fig. 4. Capacitance of a TSV with a ground tap present.

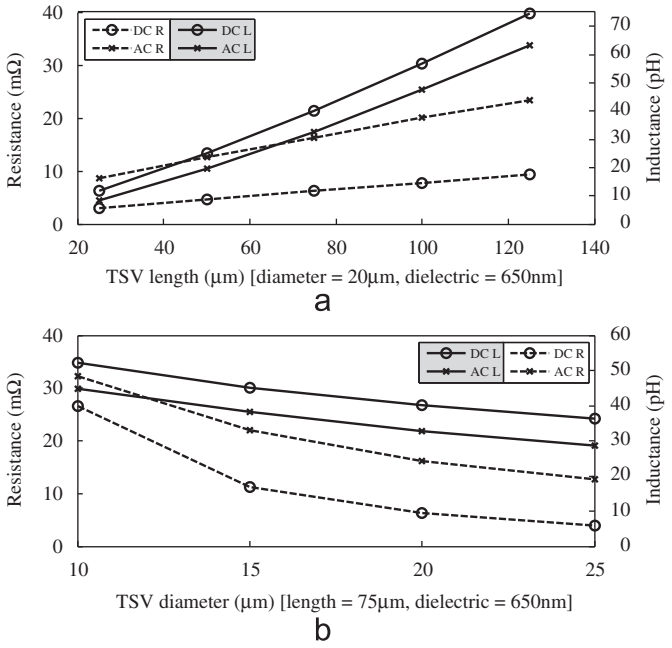

Fig. 5. Resistance and inductance of a single TSV vs. (a) TSV length and (b) TSV width.

and with the 1 μm ground plane present, the capacitance is about one-tenth the value of this upper limit, as shown in Fig. 3.

The capacitance of a TSV in the presence of a ground tap (rather than a ground plane) was also simulated. The ground tap is used to determine the worst case capacitive coupling between a TSV and a surrounding semiconductor device, where electrical field lines emanate from the TSV and terminate on the device represented as a ground tap. The ground plane provides insight on the worst case capacitance, as all field lines emanating from the TSV terminate on this ground plane. The TSV had a length of 75 μm, a diameter of 20 μm, and a dielectric thickness of 650 nm. Results are plotted in Fig. 4. The wide hatched line in Fig. 4 represents the capacitance of a TSV with the specified dimensions and a ground plane present 10 μm below. As the results indicate, the capacitance of the TSV with a ground tap replacing the ground plane is much smaller and decreases further with increasing tap distance.

In addition, the self-capacitance, the capacitance of a 3-D via with ground set at infinity, is much higher in the case where a ground tap replaces a ground plane. The self-capacitance increases from less than 0.5 to 5 fF when a ground tap is used. This implies that a larger fraction of the electrical field lines originating from the 3-D via and that once terminated on the ground plane no longer terminate on a metal conductor. These field lines are a concern with regard to the type of shielding necessary to prevent capacitive coupling.

Both the ground plane and ground tap simulations indicate that the electrical field lines originating from a 3-D via are non-negligible and must be shielded. The self-capacitance that is reported for a TSV with a ground tap is the capacitance for field lines terminating at infinity. Therefore, any interconnect or 3-D via placed at a close proximity with the aggressor 3-D via will experience a much higher coupling capacitance than the self-capacitance reported in Fig. 4. Most importantly, note that a ground tap is not sufficient to shield the electrical field lines produced by a TSV.

Once the capacitance of a single TSV was determined, the resistance and inductance was examined for the same variations in via length, width and dielectric thickness. In this case, the results for the dielectric thickness are ignored as R and L are dependent on the cross-sectional area of the via. The various dielectric thicknesses do not alter the cross-sectional area significantly, thereby leaving R and L unchanged for the dielectric thicknesses examined.

Results from this set of simulations are included as Fig. 5. The DC resistance (5–25 m Ω) and the resistance at 1 GHz (10–35 m Ω), accounting for skin effect at high frequencies, are much smaller than the resistances found in [17] (150–180 m Ω) for the SOI technology as the cross-sectional area of the bulk TSV is much larger and is filled with less resistive Cu as compared with the tungsten (W) filled vias in [6]. The inductance of a single TSV via is considered the self-inductance, or the L_{11} term. Also note that Quick 3D solves for the asymptotic values of the inductance. Therefore, Q3D does not solve for the L during the transition from the DC value to the high frequency value.

The inductance of a single 3D via in the presence of a ground tap was also simulated for increasing ground tap distance. Results indicate a negligible effect on the 3D via partial self-inductance (L_{11}). The DC and AC partial self-inductance increased by less than 0.4% and 2.8%, respectively, from the nominal 40.103 and 32.619 pH inductances extracted for a 75 μm length, 20 μm diameter, and 650 nm dielectric liner thickness 3D via over a ground plane.

The presence of a ground tap signifies the presence of a return path. As the ground tap is parallel to the 3-D via, whereas the ground plane is perpendicular, a partial mutual inductance term (L_{21}) is now present between the 3-D via and the ground tap. The L_{21} term, in addition to L_{11} and L_{22}, is used to calculate the loop inductance formed between the 3-D via and the ground tap. Results indicate that the mutual inductance between a 3-D via and a ground tap is less than 5% of both the DC and AC self-inductance of the 3-D via. More specifically, the DC mutual inductance decreases from 1.92 to 1.18 pH as the tap distance is increased from 0 to 25 μm. The AC L_{21} decreases from 1.20 to 0.74 pH for the same range of increasing tap distances. Therefore, the loop inductance is suitably estimated by adding the self-inductance of the 3-D via with the self-inductance of the ground tap.

Once the capacitance, inductance and resistance of a single TSV were determined, these values were then used to calculate RC and

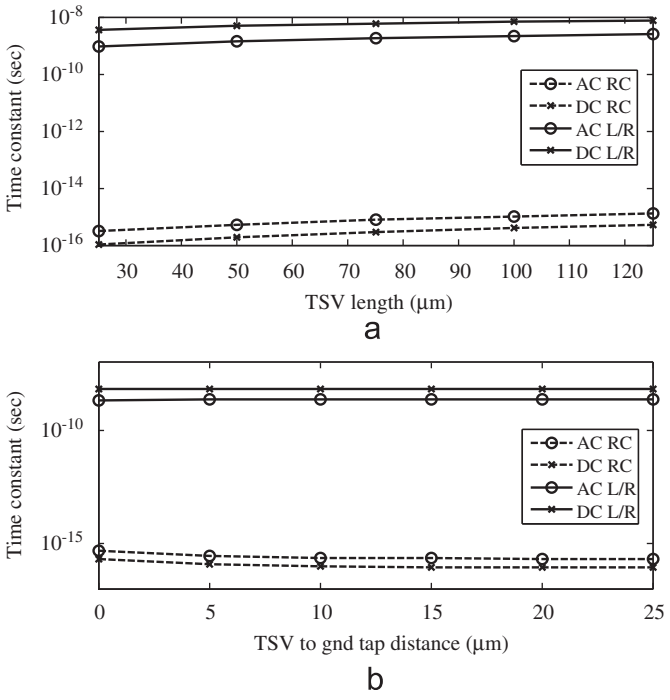

Fig. 6. *RC* and *L/R* time constants of (a) a single TSV over a ground plane and (b) a single TSV with a ground tap.

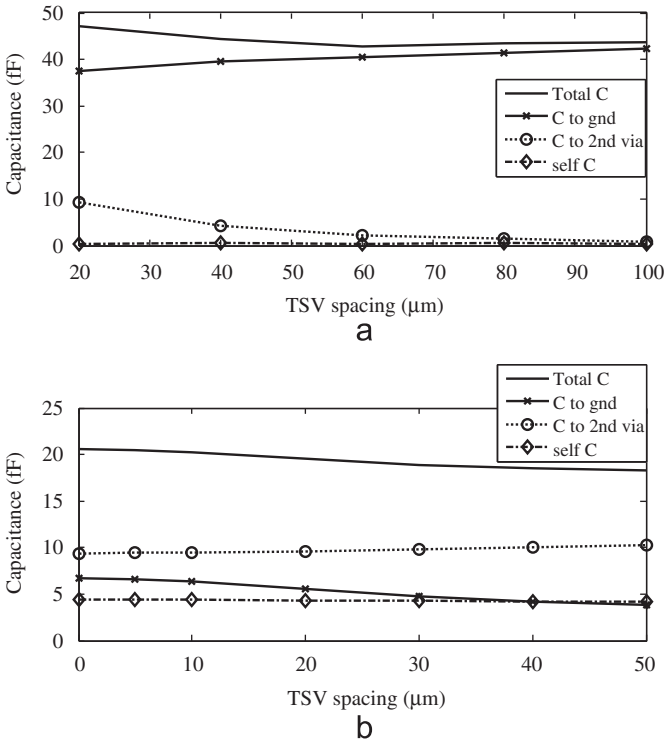

Fig. 7. Capacitance of two TSVs when (a) using a ground plane and (b) using a ground tap.

L/R time constants. Fig. 6 includes DC and high frequency *RC* and *L/R* time constants for the various lengths examined. Time constants were calculated for both a TSV over a ground plane and a TSV in the presence of a ground tap. From the figure, it is apparent that the *L/R* time constant dominates the *RC* time constant. Similar results were found for both the widths and dielectric thicknesses investigated.

With regard to the placement of the 3-D via over a ground plane or in proximity of a ground tap, the change in both the *RC* and *L/R* time constants is minimal. The *L/R* time constant does not change significantly since both the *L* and *R* values of a TSV remain about the same for both cases. However, the *RC* time constant is affected by the reduced capacitance when a ground tap replaces a ground plane. The decrease in capacitance is no more than one order of magnitude smaller when a ground tap is present, and the effect is further reduced when compared to a ground plane that is moved further from the 3-D via. The conclusion to note from examining the *RC* and *L/R* time constants is that the *L/R* time constant basically remains the same when either a ground plane or ground tap is used, whereas the *RC* time constant potentially is reduced by at most one order of magnitude. As both the ground tap and ground plane are used to characterize different electrical characteristics of a TSV, a comparison of the *RC* and *L/R* time constants provide insight of the TSV for two different environmental settings and is not used to directly compare ground taps and ground planes.

5. TSV to TSV interaction

After characterizing the electrical properties of a single TSV, the capacitive and inductive couplings between two TSVs were investigated. Understanding the capacitive and inductive noise between two vias gives insight in the type of shielding techniques necessary to assure proper signal integrity. Both the capacitive and inductive couplings were simulated for increasing via separations. In addition, the capacitance between two TSVs was examined in the case that the 1 μm thick ground plane was replaced by a 25 μm × 25 μm footprint and 10 μm deep ground tap. The ground tap was placed between two TSVs 40 μm apart (60 μm pitch), and was gradually moved further away from both vias, producing an isosceles triangle between the vias and itself.

Results examining the capacitive coupling for both the ground plane and ground tap simulations are included in Fig. 7. The placement of a ground plane nearly doubles the total capacitance as more electric field lines terminate on the ground plane at a closer proximity. However, the ground plane halves the coupling capacitance between the two TSVs as compared with the ground tap since fewer field lines terminate on the other via with the ground plane present. Finally, the TSVs that include a ground tap have much higher self-capacitances, which are field lines that do not terminate on either the other via or the ground tap.

The self-inductance (L_{11}), mutual inductance (L_{21}) and loop inductance between two TSVs are plotted in Fig. 8. Eq.(3) relates the self-inductance and mutual inductance to the loop inductance. Both Eq. (3) and Fig. 8 reveal that a higher mutual inductance, which is produced when two vias are at close proximity, reduces the total loop inductance. Fig. 8 gives insight to the loop inductance formed between two TSVs for increasing via separation, and can be used to develop guidelines for return path placement when it is necessary to reduce the loop inductance:

$$L_{loop} = L_{11} + L_{22} - 2 \times L_{21} \tag{3}$$

Using the upper bound values of inductance and capacitance, 70 pH and 50 fF, respectively, reveals a resonant frequency of approximately 85 GHz. Such a high resonant frequency indicates that only *R* and *C* can be considered for low frequency interstratum signals of hundreds of MHz.

However, inductance plays an important role in high frequency signals as well as in power grid design where $L\,\mathrm{d}i/\mathrm{d}t$ voltage droop needs to be considered.

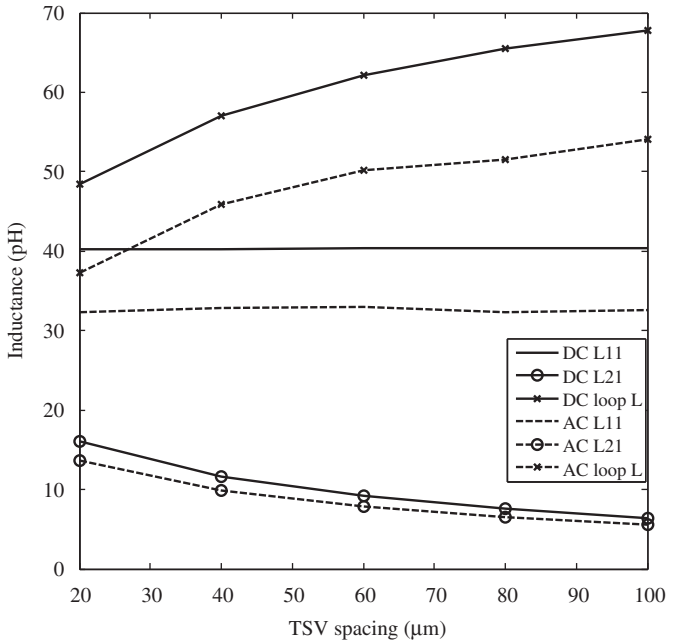

Fig. 8. Self, mutual and loop inductances of two TSVs for increasing via separation.

Table 1
Interstratum connection elements and parasitics.

Element	Critical dimensions	Parasitics
Microconnect	Footprint: 5 μm × 5 μm, height: 10 μm	R=40 m Ω, C=0.4 fF
Through-Si via	Footprint: 5 μm × 5 μm, sidewall thickness, t: 1 μm, height, h: 50 μm	R=43 m Ω, C=40 fF

6. Interstratum connection delay and power trend

Assuming that the geometry and electrical parasitics of a TSV and microconnect are as shown in Table 1, corresponding to the 90 nm technology node, we can design a 3-D IO driver circuit that is an optimally sized inverter driving the interstratum connection and a receiving inverter (Fig. 9a). Furthermore, it is desirable to scale the 3-D IO driver circuit along with the TSV footprint using a roadmap for the TSV dimensions and to predict a trend for interstratum connection power and bandwidth. In our own roadmap for TSVs, we assume a 5 um diameter via in 90 nm technology (year 2004) and scale it down accordingly per the International Technology Roadmap for Semiconductors (ITRS) technology node (critical dimension) scaling trend. The TSV aspect ratio is kept constant (10:1) over all the technology nodes, which is in agreement with the maximum TSV aspect ratio as predicted in the ITRS 2008 Interconnect Section [20]. Fig. 10 compares TSV diameters from our own roadmap used for this study with those from the ITRS 2008 Interconnect Section. Note that the TSV scales in very close agreement in the near-term (up to year 2013) followed by more aggressive scaling seen in our roadmap. Submicrometer diameter TSVs, as predicted after year 2015, require an aggressive substrate thinning process that SOI technology is better suited than bulk Si technology for manufacturing feasibility.

Next we compare the delay and power of the 3-D IO driver to that of a 1 mm long global wire segmented with repeaters, as depicted in Fig. 9b. A long global interconnect is optimally buffered by inserting properly sized repeaters or drivers at smaller interconnect segments or stages. Researchers in [3] investigated global interconnect delay in 2-D and 3-D ICs using an analytical approach for modeling interconnect and gate delay.

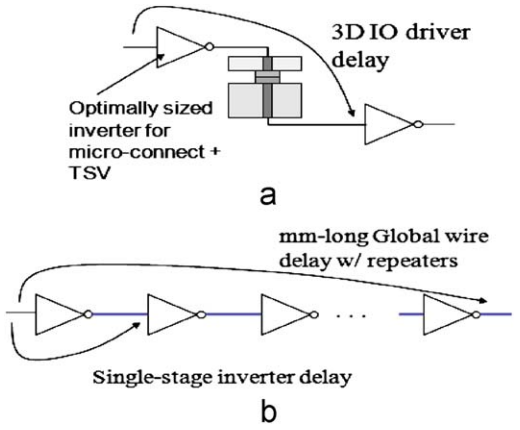

Fig. 9. Schematic illustration of a 3-D IO and global wire with repeaters for delay and power comparison.

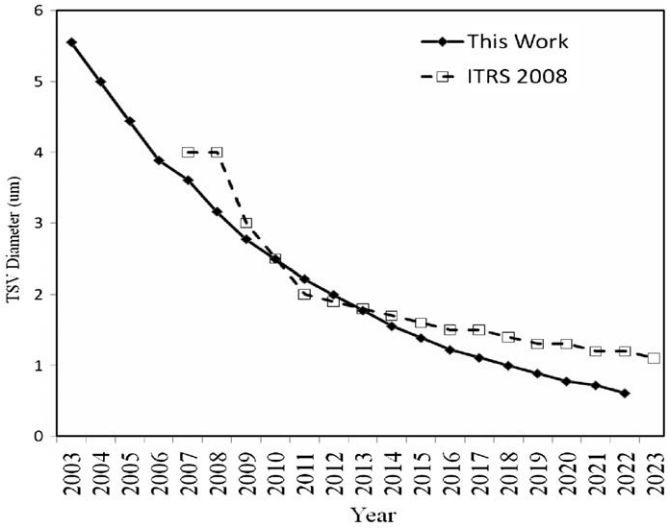

Fig. 10. Scaling trends for TSV diameters over time.

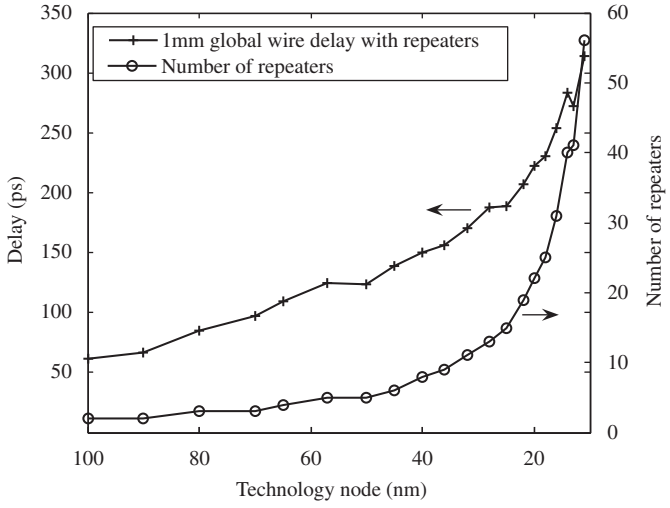

Fig. 11. Global wire delay per mm length with repeaters, and the number of repeaters.

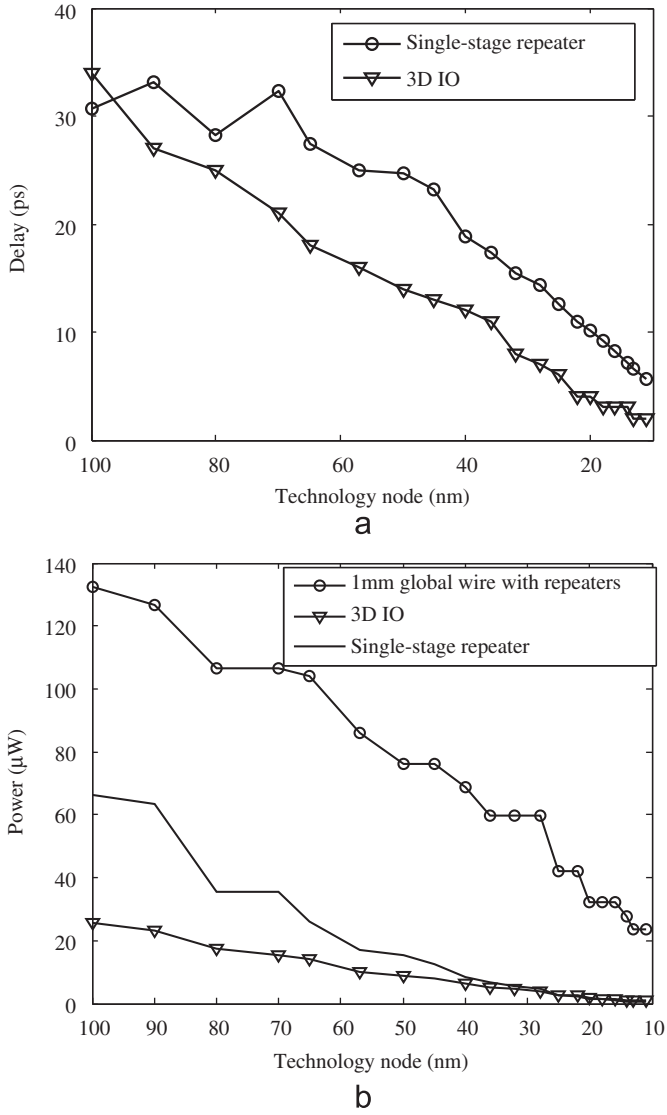

Fig. 12. 3-D IO and global (a) wire delay comparison and (b) power comparison.

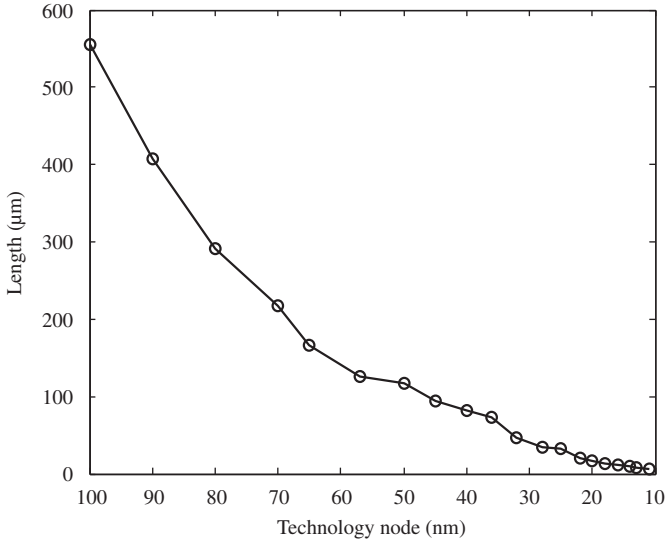

Fig. 13. 2-D global wire length for equivalent 3-D IO delay for use in 3-D layout partitioning and placement.

Using the same analytical method as in [19] and applying it to the most recent data from the International Technology Roadmap of Semiconductors (ITRS) [20], we estimated delay per mm long global wire with optimally placed repeaters and a various number of repeaters as illustrated in Fig. 11. Using data from Fig. 11, we can estimate single stage repeater delay, measured from the input of an inverter/repeater to the input of the next inverter/repeater (Fig. 9b), for each technology node. Fig. 12a shows technology node scale plots of the single-stage repeater delay and 3-D IO driver delay computed from spice simulations of Fig. 9a in 90 nm technology and scaled accordingly for each technology node. Similarly power consumption for an 800 MHz signal through the 3-D IO, the mm-long global wire, and a single-stage repeater are plotted in Fig. 12b.

According to our analysis, 3-D IO delay is smaller than even the single-stage repeater delay in a global wire while the power consumption is significantly less than the total power consumed by the global wire. The power consumption is similar to that of a single-stage repeater for scaled technologies. We also computed the global wire length necessary to produce an equivalent 3-D IO delay, and included the results in Fig. 13. The equivalent wire length can be used in physical design tools to optimally partition a 2-D circuit and place the partitions in 3-D topologies for better power and performance.

7. Conclusion

The electrical characterization of a single TSV and the coupling between two TSVs was reported. Results indicate that the capacitance can be much lower in practice with a ground plane or ground tap as compared with what is predicted by the analytical models with perfect shielding. In addition, the inductive time constant usually dominates over the capacitive time constant. A high resonant frequency indicates that inductance would play an important role in high frequency signals as well as in power grid design where $L\,di/dt$ voltage droop needs to be considered. We also analyzed a technology scaling trend of TSVs, and compared 3-D IO power and delay trends with those of global interconnects over various technology nodes. Our analysis confirms that the inter-stratum connections can be effectively utilized to increase performance with reduced power for global routing in a 3-D chip.

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