Run-Time Voltage Detection Circuit for 3-D IC Power Delivery

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***Abstract*—An advantage of 3-D integrated circuits is the possibility to integrate heterogeneous technologies on separate device planes. The device planes are fabricated in different technologies operating at distinct power supply voltages. A mechanism to detect and set the power supply voltage of each domain within each device plane of a 3-D IC is described. The detection of the power supply voltage is achieved through the placement of a ring oscillator circuit in each voltage domain. The current is supplied at the set voltage to the device plane through dedicated power modules comprising of a frequency to voltage converter and a dependent voltage source placed on a dedicated power plane. The functionality of the supply voltage detection and delivery circuits is verified through SPICE simulation of the device plane (22 nm technology) and power plane (45 nm technology). The implementation of the proposed circuits for 3-D IC design facilitate a plug-and-play approach for the integration of heterogeneous technologies.**

Keywords*—3-D integration, heterogeneous circuits, voltage detection, IC power delivery.

I. Introduction

The high power consumption and signal delay due to global interconnects in nano-scale technologies has produced research in novel integration technologies. One novel research area is through silicon via (TSV) based 3-D IC technology, where each layer or stratum is fabricated separately and subsequently vertically integrated [1]. With 3-D ICs, the fabrication of disparate strata and the final system integration are potentially completed in separate manufacturing facilities. The packaging manufacturer performing the final bonding does not necessarily need the technology dependent parameters such as voltage levels and frequency of operation for devices and IOs in each stratum. This transparency to technology information opens the possibility for *off-the-shelf* integration where dies from different foundries are bonded together by the packaging manufacturer to form a heterogeneous 3-D IC.

There are two criteria to facilitate a "plug-and-play" approach to 3-D IC integration. First, guidelines to standardize the interface circuit properties (location and electrical characteristics of IO ports and ESD protection) for each device plane must be developed and implemented. Second, the global power and clock generation circuits must meet the requirements of each stratum in the 3-D IC stack.

In this paper, a technique to address the global power generation and distribution is provided by developing a power supply voltage detection and power delivery circuit. The goal is to develop a power delivery system which senses the power supply voltage needed by each voltage domain (V_{DD_DP}) in each device plane at run time. A dedicated power plane is implemented to deliver power to all voltage domains in a 3-D stack. The power plane is capable of generating a range of voltages (ideally from 0.5 V to 5 V) to meet the power supply voltage requirements of various technology nodes. Depending upon the 3-D IC stack configuration and power budget, single or multiple power planes are interspersed between device planes. The goal is to provide power to a heterogeneous device configuration that includes CMOS, MEMS, or RFICs operating on disparate substrates not limited to Silicon or III-V technologies (GaAs, GaN, InP, etc.). The power supply voltage requirement of each domain on each device plane is detected by circuits found on the proposed power plane. The components of the circuit are described in Section II. The simulated performance of the circuit at nominal PVT is described in Section III, and conclusions are provided in Section IV.

II. Run Time Voltage Detection and Power Delivery

The voltage sense circuit is implemented using a ring oscillator. Each voltage domain within each device plane includes a ring oscillator capable of generating an output frequency F_{out} of 1 GHz when a control voltage equal to the power supply voltage V_{DD_DP} of the domain is applied. A 1 GHz frequency is an arbitrarily chosen value for the proposed circuit and is adjusted based on set standards. The goal is to select a common frequency of operation for all ring oscillators placed on different device planes in a given 3-D IC stack. The ring oscillator is the only required overhead for each voltage domain. The remaining components of the voltage sense circuit are part of the power module placed on the dedicated power plane. The placement of the components on the device and power planes are shown in Fig. 1.

The F_{out} generated by the ring oscillator propagates through TSVs to the power plane. A frequency to voltage converter (FVC) placed on the power plane generates a voltage V_{fvc} inversely proportional to F_{out}. V_{fvc} is equal to 690 mV when an input frequency of 1 GHz is applied to the FVC. The ring oscillator frequency increases until 1 GHz is reached, which is determined by comparing the FVC output voltage to a reference voltage source V_{ref} set to 690 mV. A voltage controlled voltage source (VCVS) supplies the control voltage to the ring oscillator. The VCVS is controlled by a voltage comparator, comparing the V_{fvc} with V_{ref}. Dedicated power modules comprising of the FVC and the VCVS facilitate point of load power delivery which offers three distinct advantages [2]: 1) Reduced noise due to a reduction of the parasitic impedance of the power distribution network as the voltage source is closer to the load circuit, 2) supply of different

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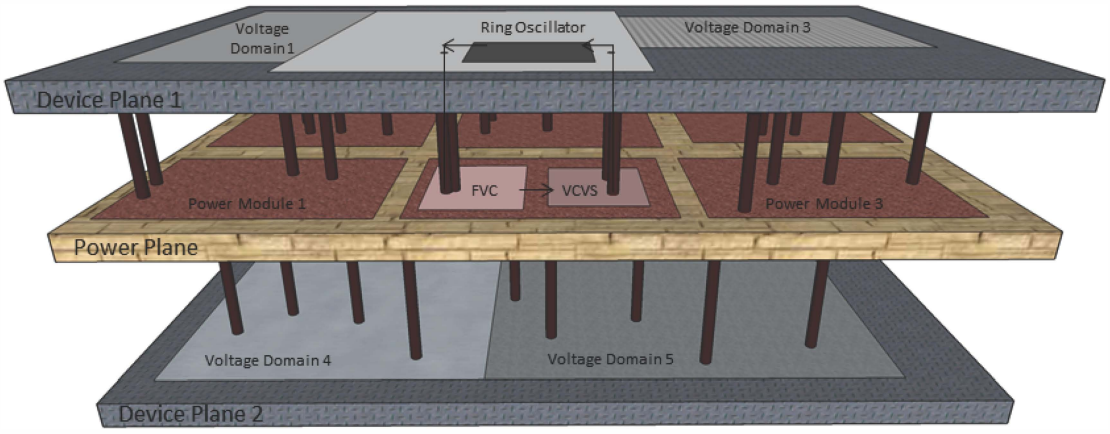

Fig. 1. The proposed voltage sense and power delivery system for 3-D ICs. A 3-D stack with device planes containing multiple voltage domains are served by a power plane consisting of multiple power modules. Each power module consists of a voltage controlled voltage source (VCVS) controlled by voltage generated from a frequency to voltage converter (FVC). The ring oscillator placed in each voltage domain provides the controlling frequency to the FVC.

voltages to heterogeneous circuits, and 3) finer granularity for voltage control.

The circuit structure and operation of all the components included in the voltage sense and power delivery circuit are described in Sections II-A through II-C. Circuits are designed with 45 nm and 22 nm PTM models [3] for, respectively, the power plane and device plane.

A. Ring oscillator circuit for individual voltage domains

Ring oscillators (RO) are widely used as voltage controlled oscillators (VCO) in high performance integrated circuits as the fundamental block for frequency synthesizers, clock recovery circuits, and clock distribution networks. The application of ring oscillators is not limited to VCOs, as ROs are used for on-chip thermal sensors [4], [5] and test structures to measure process variability [6]. The versatility of a RO is attributed to a simple CMOS implementation with no passive components, which reduces the occupied silicon area. The output frequency is stable in the presence of process, voltage, and temperature variation (PVT) and the applied control voltage.

Several ring oscillator circuit topologies are examined which provide a steady frequency reference for the detection of the targeted V_{DD_DP} of a given voltage domain. The selected ring oscillator circuit topology must provide a large frequency range when the applied control voltage varies from V_{DD_DP}/2 to V_{DD_DP} and a minimum variation in frequency due to sensitivity to PVT. A current starved RO with an output switching inverter (shown in Fig. 2) provides the best frequency stability in terms of temperature variation (less than 2%), a low phase noise of 0.06 radians, and frequency sensitivity to power supply variation of less than 10% [7], [8]. An addition based current source [9], which maintains a constant total current across process variations, is used as a header and footer circuit for the CMOS inverters cascaded to form a ring oscillator in [10]. Despite the stability of the output frequency with process variation and device mismatch, the ring oscillator topology in [10] is not suitable for the problem addressed in this paper due to the following reasons:

1) The control voltage V_{GS} to the gate of the transistor M1 must be higher than the threshold voltage V_{TH} and lower than V_{DD} for the addition based current source footer circuit shown in Fig. 3 [9]. For nanoscale technologies, where the difference between V_{TH} and V_{DD} is not large, the operating range of V_{GS} is limited, which implies a narrow voltage range for the controlling current feeding the current starved inverters.
2) A single voltage that serves as both V_{DD} and the control voltage to the inverter stages is preferred, however, the current design includes two separate voltages.

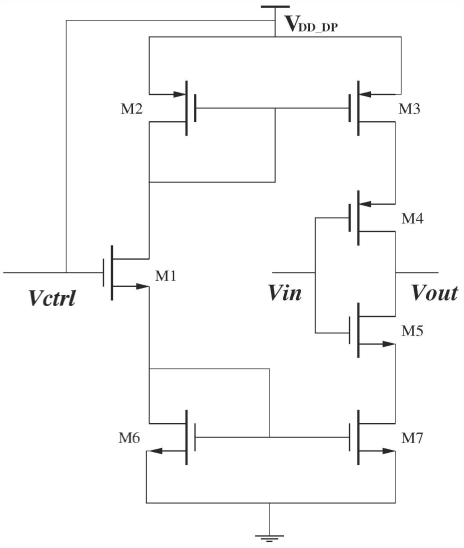

Fig. 2. A current starved and output switching inverter [7].

The current starved topology with an output switching inverter is therefore selected as the building block to implement the ring oscillator. The control voltage V_{ctrl} is applied to both the control transistor M1 and V_{DD_DP} as shown in Fig. 2. The RO circuit is implemented using a 22 nm high-performance (HP) PTM model [3], [11] with a V_{DD_DP} of 0.8 V. An output frequency of 1 GHz is achieved with three current starved inverting stages each with transistor W/L ratios ranging between 8 to 10. None of the transistors are minimum sized to reduce the impact of line-edge roughness and random dopant fluctuations which cause significant variation in the V_{TH} in

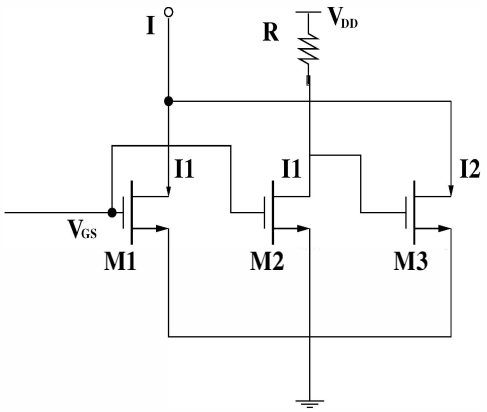

Fig. 3. Addition based current source used as footer circuit in [9].

the subnanometer technology nodes [11].

The V_{TH}, low-field mobility, and effective channel length are the three main parameters impacted by lithographic variation, stress, and doping concentration in strained silicon technology. The impact of process variation on the output frequency of the ring oscillator is evaluated with Monte Carlo analysis. A typical corner is simulated for statistical variation of V_{TH}, channel length, and mobility considering both process variation and device mismatch. The ring oscillator frequency variation with V_{TH}, channel length, and MOSFET low-field mobility is shown, respectively, in Figs. 4(a), 4(b), and 4(c). The corresponding ratio of the variance to the mean (σ/μ) for V_{TH}, the effective channel length, and the low-field mobility as percentage is, respectively, 11.9%, 5.64%, and 6.12%. The designed ring oscillator therefore exhibits moderate deviation in output frequency with process variation. The power module on the power plane that detects the ring oscillator frequency is designed to compensate for deviation from the 1 GHz target frequency due to PVT variation to ensure reliable detection and setting of the power supply voltage.

B. Frequency to voltage converter circuit

The output from the ring oscillator on the device plane is connected to a FVC circuit placed on the dedicated power plane. The connection between the ring oscillator and the FVC is through TSVs. With careful floorplanning and the development of 3-D IC interface circuit standards, the vertical alignment of the ring oscillators and the FVC circuits on the respective device and power planes ensures minimum electrical degradation of the frequency signal in terms of induced jitter and propagation delay. The circuit chosen to implement the FVC is described in [12]. The FVC operates based on charge redistribution between two switching capacitors. The generated output voltage is linearly related to the input frequency and does not require filtering to remove AC ripples, which is a common limitation with other FVC implementations using low pass filtering techniques or digital counters. The circuit implementation is area efficient, as a limited number of components are required. The FVC circuit is implemented using a 45 nm low-performance (LP) PTM model [3] with the power supply voltage V_{DD_PP} set to 1 V. The circuit implementation of the FVC is shown in Fig. 5 [12]. The current source is set to 20 μA. The capacitors C_1 and C_2 are each 10 fF and are implemented as MOSCAPS to reduce the occupied silicon area. The voltage

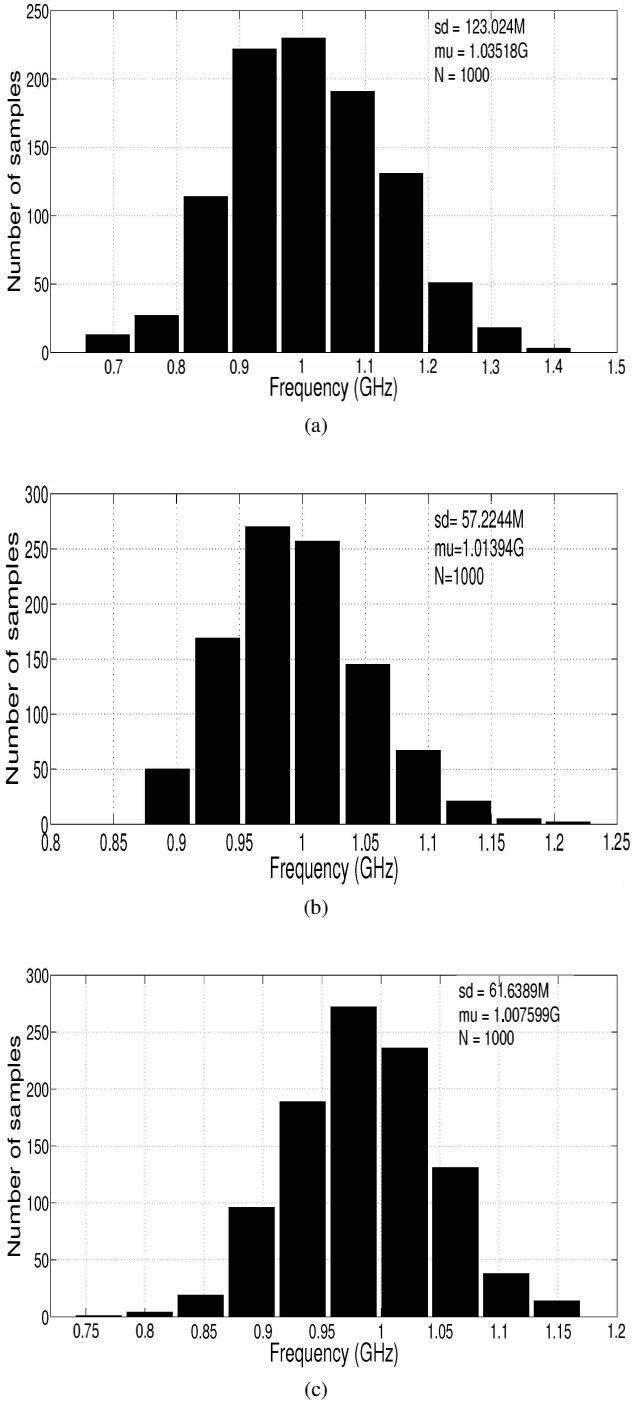

Fig. 4. Statistical variation of the 22 nm ring oscillator output frequency for (a) V_{TH}, (b) effective channel length, and (c) low-field mobility.

across the capacitors is inversely proportional to the frequency of the input signal and corresponds to a voltage of 690 mV when the input frequency is 1 GHz.

C. Voltage controlled voltage source implementation

The control voltage (V_{ctrl}) and power supply voltage (V_{DD_DP}) of the RO in the device plane are provided by a voltage controlled voltage source (VCVS) which is part of the power module in the power plane. The VCVS consists of a voltage comparator and a current source which charges a capacitor *C* (shown in Fig. 6). The charging of the capacitor

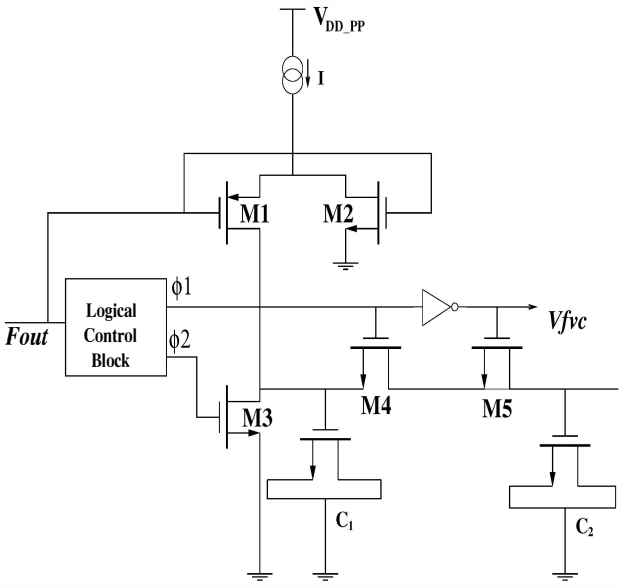

Fig. 5. Frequency to voltage converter circuit for the device plane power supply voltage detection [12].

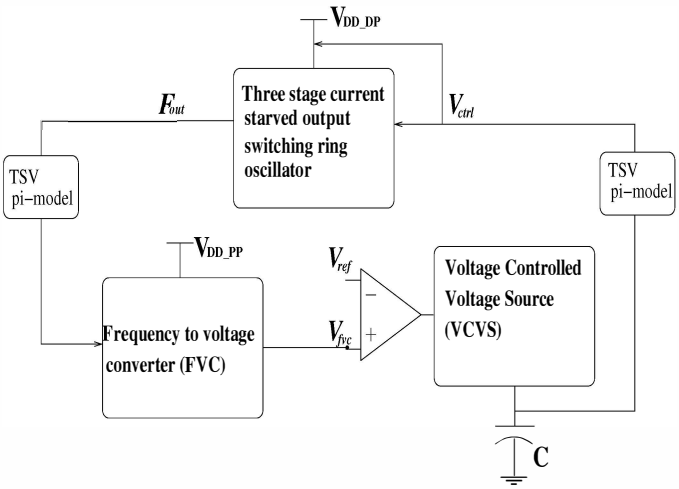

Fig. 6. Block level view of the voltage detection and power delivery circuit for 3-D IC.

through the current source is controlled by the output of the voltage comparator. The VCVS is implemented using the 45 nm thick oxide PTM model available through the NCSU 45 nm PDK [13]. The current source is designed to generate stable output voltages upto 3 V, which is sufficient to serve analog and IO devices implemented in subnanometer technologies. It is possible to generate output voltages upto 5 V by selecting an older technology node (greater than 65 nm) to implement the current source on the dedicated power plane. By supplying voltages from 0.5 V to 5 V, a wide range of disparate technologies are integrated to form a 3-D system.

The ring oscillator generates distinct frequencies when the input control voltage lies between V_{DD_DP}/2 and V_{DD_DP}. The FVC responds to these frequencies by generating an output voltage inversely proportional to the input frequencies. The varying output voltage from the FVC is constantly compared to V_{ref}. When V_{fvc} is equal to or less than V_{ref}, the comparator output becomes active low and stops the charging of the capacitor *C* through the current source, as shown in Fig. 6.

III. Simulation results

The three circuit blocks, which include the 22 nm three stage current starved output switching ring oscillator circuit on the device plane (power supply voltage V_{DD_DP} of 0.8 V), the 45 nm FVC circuit (power supply voltage V_{DD_PP} of 1 V), and the 45 nm VCVS, are simulated together. The simulation also includes the impedance of the TSVs. The connectivity of the circuit blocks is shown in Fig. 6 and the transient response is shown in Fig. 7. Assuming a vertical alignment between the power module on the power plane and the ring oscillator on the device plane, the interconnect length is negligible and is not considered in the simulation.

The control voltage from the VCVS and the output signal of the ring oscillator propagate through TSVs. The impact of the TSVs [14], [15] is incorporated by using an equivalent *RC* pi-model. The values of the DC resistance (505.8 mΩ), 1 GHz resistance (570.72 mΩ), and capacitance (8.7 fF) of a single TSV are computed from the closed form expressions developed in [16]. The pi-model represents a Tungsten filled TSV with a length of 16 μm, diameter of 1.5 μm, and dielectric thickness of 0.25 μm. Each *RC* pi-model shown in Fig. 6 represents two TSVs in parallel.

The transient response of the 22 nm ring oscillator (F_{out_22nm}), the FVC output voltage (V_{fvc}), and the control voltage generated by the VCVS block (V_{ctrl_22nm}) is shown in Fig. 7. The ring oscillator is the only load element served by the power module for the transient simulation. The VCVS transient simulation therefore excludes the impact of load transients and resistive losses due to the power delivery network and additional load circuits. The desired power supply voltage of 0.8 V is reached in less than 80 ns. The proposed voltage detection and power delivery circuit is further tested to provide the power supply voltage to a 45 nm device plane. A three stage current starved ring oscillator is designed using a 45 nm LP PTM model (V_{DD_DP} of 1 V). The VCVS is able to reliably generate a control voltage of 1 V (V_{ctrl_45nm}) in less than 100 ns, as shown in Fig. 7(c).

IV. Conclusions

A mechanism to detect the power supply voltage of a given voltage domain in a 3-D IC is implemented by placing a ring oscillator in each domain located on disparate device planes. The chosen circuit topology for the ring oscillator exhibits acceptable deviations due to PVT variations in a 22 nm technology. A σ/μ ratio (as a percentage) of 11.9%, 5.64%, and 6.12% is determined for, respectively, threshold voltage variation, channel length variation, and low-field mobility. The power requirement of each voltage domain is served by a single power plane that includes multiple point of load power modules, with each module consisting of a voltage controlled voltage source regulated by a frequency to voltage converter. The power supply voltage detection and delivery mechanism is demonstrated by simulating the device plane and power plane in two different technology nodes. The targeted power supply voltage for both the 22 nm and 45 nm device planes is detected and set in less than 100 ns, as shown through simulation.

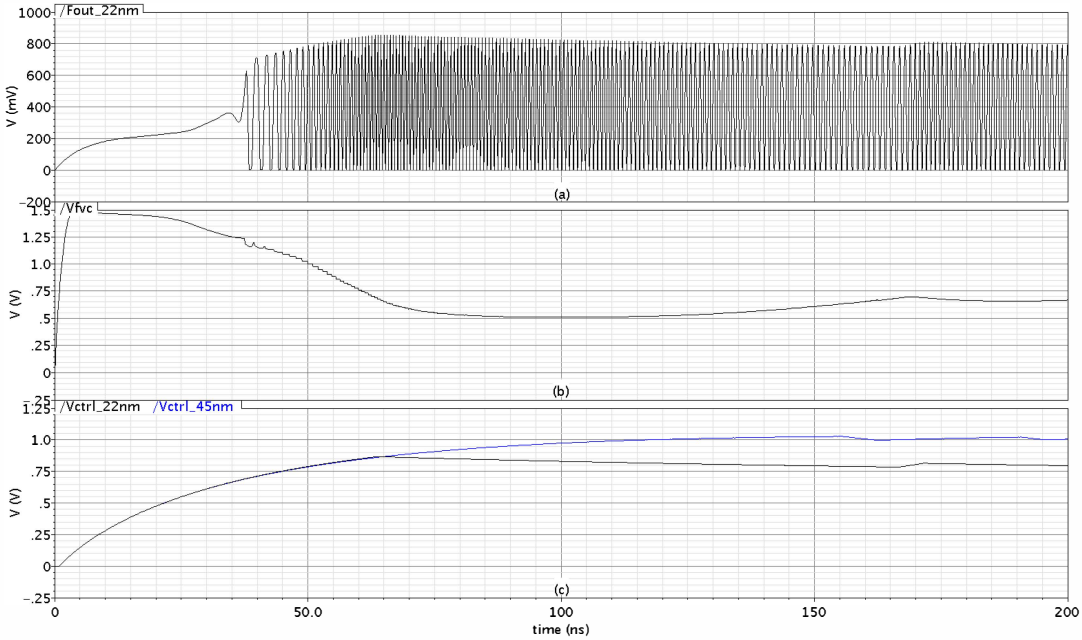

Fig. 7. Transient response of the (a) ring oscillator placed in a 22 nm device plane, (b) FVC, and (c) control voltage generated from the VCVS for both a 22 nm (V_{DD_DP} of 0.8 V) and 45 nm device plane (V_{DD_DP} of 1 V).

REFERENCES

[1] I. Savidis, *Characterization and Modeling of TSV Based 3-D Integrated Circuits*, Ph.D. Thesis, University of Rochester, 2013.

[2] S. Kose and E. G. Friedman, "Distributed on-chip power delivery," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, No. 4, pp. 704–713, December 2012.

[3] Nanoscale Integration & Modeling Group Arizona State University, "Predictive Technology Model (PTM)," http://www.eas.asu.edu/~ptm.

[4] F. Kashfi and J. Draper, "Thermal sensor design for 3D ICs," *IEEE 55th International Midwest Symposium on Circuits and Systems*, pp. 482–485, August 2012.

[5] S. Lopez-Buedo, J. Garrido, and E. Boemo, "Thermal testing on reconfigurable computers," *IEEE Design & Test of Computers*, Vol. 17, No. 1, pp. 84–91, March 2000.

[6] J. S. Panganiban, "A ring oscillator based variation test chip," M.S. Thesis, Massachusetts Institute of Technology, 2002.

[7] G. Jovanovic, M. Stojcev, and Z. Stamenkovic, "A CMOS voltage controlled ring oscillator with improved frequency stability," *Scientific Publications of the State University of Novi Pazar, Series A: Applied Mathematics, Informatics and Mechanics*, Vol. 2, No. 1, pp. 1–9, December 2010.

[8] A. Ramazani, S. Biabani, and G. Hadidi, "CMOS ring oscillator with combined delay stages," *AEU-International Journal of Electronics and Communications*, pp. 515–519, May 2014.

[9] X. Zhang, A. M. Pappu, and A. B. Apsel, "Low variation current source for 90nm CMOS," *IEEE International Symposium on Circuits and Systems*, pp. 388–391, May 2008.

[10] X. Zhang and A.B. Apsel, "A low-power, process-and-temperature-compensated ring oscillator with addition-based current source," *IEEE Transactions on Circuits and Systems*, Vol. 58, No. 5, pp. 868–878, May 2011.

[11] Y. Cao, *Predictive Technology Model for Robust Nanoelectronic Design*, Springer, 2011.

[12] A. Djemouai, M. Sawan, and M. Slamani, "High performance integrated CMOS frequency-to-voltage converter," *Proceedings of the Tenth International Conference on Microelectronics*, pp. 63–66, December 1998.

[13] North Carolina State University, "FreePDK45," http://www.eda.ncsu.edu/wiki/FreePDK.

[14] I. Savidis and E. G. Friedman, "Electrical modeling and characterization of 3-D vias," *IEEE International Symposium on Circuits and Systems*, pp. 784–787, May 2008.

[15] I. Savidis, S. M. Alam, A. Jain, S. Pozder, R. E. Jones, and R. Chatterjee, "Electrical modeling and characterization of through-silicon vias (TSVs) for 3-D integrated circuits," *Microelectronics Journal*, Vol. 41, No. 1, pp. 9–16, January 2010.

[16] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873–1881, September 2009.