Power Supply Voltage Detection and Clamping Circuit for 3-D Integrated Circuits

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***Abstract*—A circuit that detects and sets the power supply voltage of a given device plane in a 3-D IC is proposed. The circuit consists of 1) a ring oscillator in each voltage domain located in each device plane, and 2) a power module placed in a dedicated power plane. The power module consists of four components; a divide-by-40 clock divider, a frequency detector, a voltage ramp generator, and a voltage peak detector circuit. The power module provides a stable reference voltage equal to the power supply voltage of the targeted voltage domain in the device plane. SPICE simulations of the circuit indicate that power supply voltages of less than 1 V are successfully set and provided as a reference to an on-chip voltage regulator within 500 ns and with reference voltage variation of less than 1%. The power module is integrated with on-chip voltage regulators which require a precise voltage reference. The proposed implementation permits dynamic voltage and frequency scaling and point of load power delivery.**

***Index terms*—3-D IC power delivery, voltage regulation.**

I. Introduction

Through silicon via (TSV) based 3-D integrated circuits (IC) permit the integration of heterogeneous technologies with CMOS. The integrated system may include RF, analog, micro-/nano-electromechanical systems (MEMS/NEMS) as well as emerging technologies such as nano-FET and graphene-based device planes. The design and fabrication of these disparate device planes may take place at separate facilities. Unless technology specific information on each device plane is provided, the packaging facility carrying out the final 3-D integration of the device planes is unaware of the power supply voltage requirements of the different ICs [1].

In this paper, a universal power plane that includes circuits capable of detecting the power supply voltage requirement of each device plane in the 3-D IC stack is proposed. The universal power plane consists of multiple on-chip voltage regulators serving the power needs of each voltage domain in each device plane of the 3-D stack. This arrangement facilitates point-of-load power delivery through the use of TSVs. The shorter path between the power source and load leads to both lower *IR* drop and parasitic impedance of the power distribution network [2]. Each dedicated voltage regulator for a given voltage domain facilitates dynamic voltage and frequency scaling (DVFS). 3-D IC interface guidelines are required to successfully implement this circuit, and must include specifications for the location of ports for power, clock, and signal delivery for each device plane of the 3-D IC stack [1]. The components of the power supply voltage detection and clamping circuit are described in Section II. The simulation results for two device planes are discussed in Section III. Some conclusions and ongoing work are provided in Section IV.

II. Device plane power supply detection and clamping

The block diagram of the various components of the 3-D IC supply voltage detection and clamping circuit are shown in Fig.1. Each voltage domain in the device plane consists of a ring oscillator with a current-starved output switching stage [3]. The ring oscillator operates at a frequency of 1 GHz when the applied control voltage equals the power supply voltage of the given domain. The oscillation frequency of 1 GHz is selected as it is easy to achieve with minimum current starved inverter stages in a deep sub-micron CMOS technology as well as in GaAs based RF circuits [4]. The power module that serves a voltage domain consists of a clock divider, frequency detector, voltage ramp generator, voltage peak detector, and a voltage regulator.

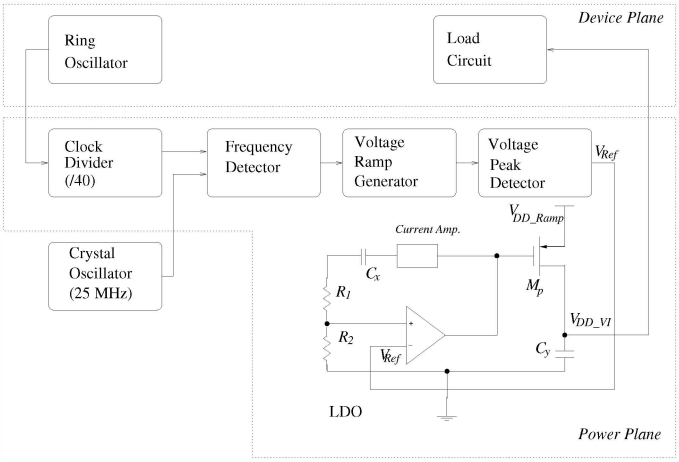

Fig. 1. Block diagram of the power supply voltage detection and clamping circuit depicting a single voltage domain in one device plane and the corresponding power module in the power plane.

The ring oscillator output frequency is down converted by a factor of 40 by a clock divider consisting of a divide-by-8 cascaded together with a divide-by-5 circuit block [5]. A frequency comparator compares the output of the clock divider with a 25 MHz clock source (off-chip crystal oscillator). The frequency comparator is implemented using four D-FFs as shown in Fig. 2(a). The frequency comparator is chosen over a phase frequency detector (PFD) as the PFD generates UP and DOWN signals (due to D-FF clock-to-Q delay) even when the inputs are phase locked [6]. In addition, the voltage detection circuit does not require that the down converted ring oscillator frequency is matched in phase with the 25 MHz reference signal.

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A voltage ramp generator circuit (RGC) includes a constant current source charging a capacitor C_1 and a switch S_1 that controls the duration of the ramp voltage, as shown in Fig. 2(b). The UP and inverted DOWN signal are logically ANDed together ($UP \bullet \overline{DOWN}$) to generate the control signal for S_1. When the 3-D IC is first powered on, the ramp generator provides an initial voltage to the ring oscillator, and the UP signal from the frequency detector is high as the down converted frequency from the ring oscillator is less than 25 MHz. The frequency increases as the ramp generator output voltage increases. When the ring oscillator reaches the 1 GHz frequency, the UP signal is de-asserted and any further increase in frequency asserts the DOWN signal. The switch S_1 is in the open state, preventing any further increase of charge (and therefore voltage) on C_1. The voltage V_{RGC} on C_1 corresponds to the power supply voltage of the voltage domain (V_{DD_VI}) in which the ring oscillator is placed. The discharging of the capacitor C_1 through the load circuit causes the ring oscillator frequency to drop below 1 GHz, which re-asserts the UP signal and places S_1 in the closed state. The UP signal continues to periodically toggle ensuring that the voltage V_{RGC} is maintained at the desired level.

The variations in V_{RGC} due to discharging of the capacitor C_1 are filtered using a voltage peak detector circuit (shown in Fig. 2(c)). The peak detector circuit consists of a PMOS M_1 which controls the current charging the capacitor C_2. A voltage comparator compares the output voltage V_{Ref} across the capacitor C_2 with V_{RGC}. The output voltage from the comparator biases M_1. V_{Ref} follows the positive transition of V_{RGC} and at steady state equals the maximum value of V_{RGC}. The peak detector circuit therefore provides a steady voltage reference with less than 1% ripple voltage variation from the targeted power supply voltage of the device plane (V_{DD_VI}). V_{Ref} is used as the reference voltage for the voltage regulator serving the load circuit in the device plane. On-chip voltage regulator topologies like the LDO and buck converter are suitable for integration with the proposed voltage detection and clamping circuit. The stable reference voltage provided by the proposed circuit ensures superior line regulation offered by the voltage regulator.

III. Simulated Circuit Results

Two device planes are simulated using the 45 nm low-performance (V_{DD_VI} of 1 V) and 22 nm high-performance (V_{DD_VI} of 0.8 V) predictive technology models (PTM) [7]. The designed ring oscillators for each device plane include three inverter stages in a current starved output switching configuration. The design is robust against threshold voltage variation, channel length variation, and low-field mobility variation [8].

The components of the power module are implemented with the 45 nm PTM models. The divide-by-40 clock divider and frequency detector circuits are simulated using the 45 nm low-performance PTM model (V_{DD_PP} of 1 V). The voltage ramp generator and peak detector circuits are implemented using the 45 nm thick oxide (V_{DD_Ramp} of 3 V) PTM model. A DC-DC level shifter is used to convert the UP and DOWN signals from a V_{DD_PP} of 1 V to a V_{DD_Ramp} of 3 V. The slope of the voltage ramp signal is deliberately kept low (0 V to 3 V in 2 µs) to ensure stable operation. The mimimum

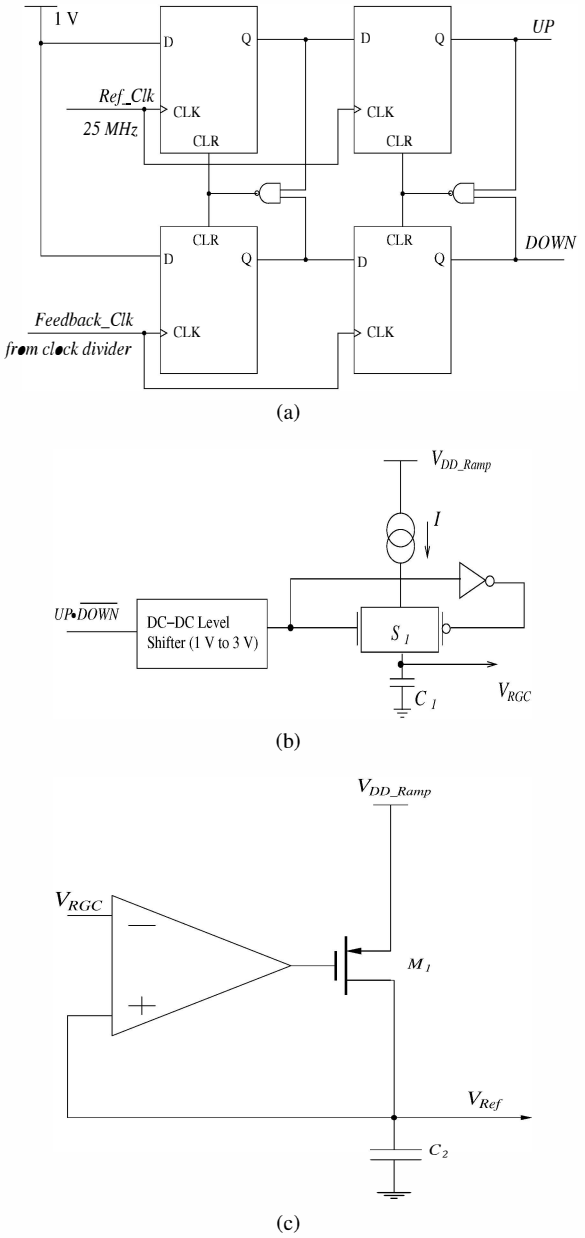

Fig. 2. Circuit schematic of (a) frequency detector, (b) voltage ramp generator, and (c) peak detector.

voltage detected reliably by the power module is 0.7 V. The maximum voltage provided by the ramp generator is 2.5 V. SPICE circuit simulations indicate a maximum variation of 1% in the reference voltage V_{Ref} provided to the on-chip voltage regulator for V_{DD_VI} of less than 1 V. This is comparable to the stability of reference voltages used by off-chip buck converters, where approximately 1% variation is currently achieved [9].

The simulation results for detecting and clamping the power supply voltage for a voltage domain in a 22 nm device plane are shown in Fig. 3. V_{Ref} reaches V_{DD_VI} of 0.8 V in 370 ns. The detection and clamping circuits on the 45 nm device plane require 420 ns for V_{Ref} to reach the target voltage V_{DD_VI} of 1 V. The proposed circuit therefore offers a fast transition to the desired power supply voltage level at startup and is suitable for integration with on-chip voltage regulators.

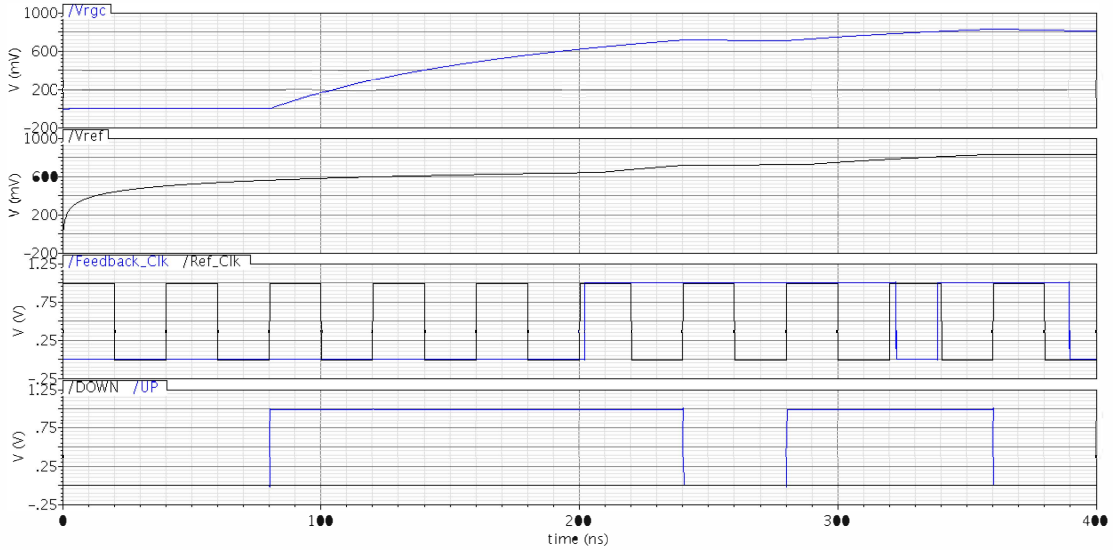

Fig. 3. Analysis of the power supply voltage detection and clamping circuit for a 0.8 V domain in a 22 nm technology.

IV. Conclusions

A circuit to detect and reliably set the power supply voltage of a given voltage domain in a 3-D IC is described. All components except for a ring oscillator are part of the power module located in a separate and dedicated 45 nm power plane. Multiple power modules serve as point of load voltage delivery circuits to the different device planes. Correct power supply voltage detection and clamping is demonstrated through circuit simulation for two device planes, one in 22 nm and the other in 45 nm. The power module is capable of setting the power supply voltage of a device plane ranging from 0.7 V to 2.5 V. The precise voltage generated from the power module acts as a reference voltage for an on-chip LDO or buck converter. The reference voltage is within 1% of the targeted power supply voltage, as indicated by simulated results.

Further work is planned to test the precision of the generated reference voltage through statistical analysis of multiple PVT corners. The effect of the interconnect and the TSVs will be included to provide a comprehensive analysis of the 3-D IC power detection and delivery circuit.

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