A Quasi-Analytic Behavioral Model for the Single-electron Transistor for Hybrid MOS/SET Circuit Simulation

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***Abstract*— A methodology to incorporate single-electron transistors (SET) into the IC design flow is introduced in this paper. A SET model is developed that is defined as a VERILOG-A module that can be used for SPICE-like simulation of hybrid circuits containing SET and MOS transistors. The SET model is formulated in a semi-symbolic form, which provides insight and intuition on the functionality of the device. The model was verified on a SET-only and hybrid (SET and MOS transistors) implementation of an inverter. The proposed model is compared with a verified analytical model that applies a master equation, which results in errors of approximately 1.6% for a SET-only inverter and 1.3% for a hybrid inverter.**

I. INTRODUCTION

Many emerging technologies including SET, memristors, and spintronics are possible candidates to form hybrid circuits with MOS devices. Electrical simulation of hybrid systems is a challenging task as models for emerging devices are not always available.

Specifically, hybrid SET/MOS circuits integrate the mature IC design flow of MOS with the novelty of SET-electronics (also denoted as single-electronics). The simulation of MOS circuits is based on long-established tool frameworks including SPICE, electromagnetic simulators, and verification methods. As a result, to accurately and effectively simulate single-electronics in a hybrid MOS/SET circuit, simulation frameworks are needed compatible with SPICE.

Currently, there are three primary techniques to simulate SET circuits, which include: 1) Monte Carlo techniques (MC), 2) Master Equation approaches (ME), and 3) Macro Model methods (MM). The MC technique yields high accuracy in describing systems based on tunnel junctions [1]. The MC approach, however, is limited by the high computational cost when modeling large circuits and does not allow for the simulation of hybrid circuits. The ME approach applies a Markov process in order to develop a mathematical expression that describes the tunneling of an electron traveling from one island to another. There is a trade-off between obtaining a more accurate outcome and the complexity of the developed equation [2]. The MM approach describes the SET using passive and active circuit elements. However, a limitation of the MM technique is the lack of scalability [3].

The proposed simulation methodology makes use of the greater accuracy obtained through SIMON –a device-level simulator [1] in order to generate the electrical characteristics of a SET, which are expressed as mathematical equations that best fit the initial simulation data. To provide further utility as a SPICE-like simulator, the resulting mathematical equations of the SET device were translated into an equivalent behavioral model.

In this paper, the methodology for hybrid simulation is described in Section II. A quasi-analytic model is developed in Section III. A hybrid circuit is simulated using the developed model, with results provided in Section IV. Some concluding remarks are provided in Section V.

II. MODELING METHODOLOGY

The approach to model and simulate SET/MOS hybrid circuits is summarized in Fig. 1. There are three stages to the simulation of SET/MOS hybrid circuits: 1) modeling the structure of the SET, 2) defining a functional model based on user-defined or library models, and 3) developing behavioral model that defines the structure of a standard circuit simulator.

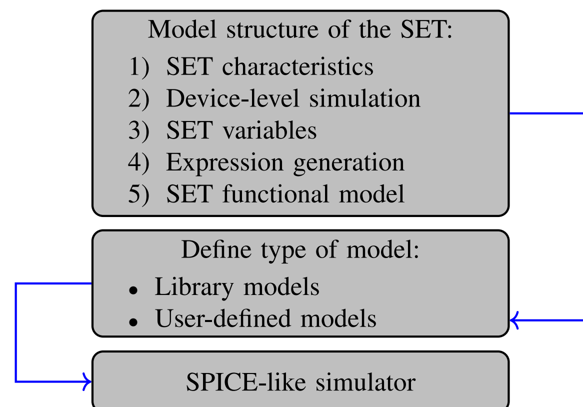

Fig. 1: Modeling methodology for the simulation of hybrid SET/MOS circuits.

For the model of the SET (first stage), the type and range of variables is defined. Device-level simulations are completed to analyze the IV characteristics of the SET transistor. Based on simulation, the characteristics of the drain current as a function of the selected variables are described. From the device-level results and the determined

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IV characteristics, a mathematical expression is developed. A curve-fitting technique is applied to the simulation data to determine the values of the fitting parameters of the mathematical expression, which account for shifts in amplitude and displacement due to Coulomb Blockade. The mathematical expression represents a user-defined functional model of the SET.

III. Formulation of the Model

A. Previous Work

In this section, the formulation of the model using the methodology proposed is described. In subsection A, symbolic relationships for the frequency and the phase parameter of the SET are included them in the model. In subsection B, a curve-fitting approach is implemented for the remainder parameters.

In prior work, symbolic relationships that include the drain voltage (V_{DS}), the gate and tunnel capacitance (C_G, C_{TS}, C_{TD}), and the background charge (q_{BC}) have been reported [4]. The electric parameters are related to the frequency and the phase as given by, respectively,

$$f = \frac{2\pi C_G V_{GS}}{e}, \text{ and} \tag{1}$$

$$\phi = \pi - q_{BC} - \frac{\pi V_{DS} \left(C_G + C_{TS} - C_{TD}\right)}{e}. \tag{2}$$

In [5], for the case when both tunnel junctions have the same value, the tunnel resistance takes a symbolic form for the symmetric SET, as given by R_T in

$$I(V_{GS}, R_T) = (A \cdot \cos(f \cdot V_{GS} + \phi) + D) \cdot \frac{1 \times 10^8}{R_T}. \tag{3}$$

The frequency obtained using (1) is the same as reported in [6]. As a result, the modeling methodology proposed in this work provides a pseudo-analytic expression of a SET that has been validated with prior work. In other words, the model developed here is in part symbolic based on physical and electrical parameters and part approximate. In addition, other variables of the SET including the amplitude, displacement, and warping parameters are integrated into the model.

B. Proposed Model

The proposed SET model is given as

$$y = A \cdot W\left(\cos\left(f \cdot x + \phi\right)\right) + D, \tag{4}$$

where A, W, f, ϕ, and D are respectively, the amplitude, warping, frequency, phase, and displacement parameters. The non-linear function W represents a warping in the sinusoidal function. The dependent variable, y, represents the drain current, and the independent variable, x, is the gate-to-source voltage. What follows is an outline of the methodology applied in the paper.

1) SET variables: The variables characterizing the SET are defined and selected. For the SET, four sets of variables are applied that account for electric, design, process, and environmental parameters as shown in Fig. 2. A curve-fitting technique is used to include the V_{DS}, C_G, and C_T variables, which are directly related to the amplitude and the displacement parameters. In addition, the symbolic approach relates the electric, design, and process variables through the frequency and phase parameters given in (1) and (2), respectively. The environmental variable and asymmetric tunneling resistances (R_T) are not included in the model.

2) SET characteristics: The I_{DS} as a function of V_{GS} is characterized analytically for V_{DS} values of $\pm 20mV$. The C_Σ parameter is included to account for the capacitance of the SET.

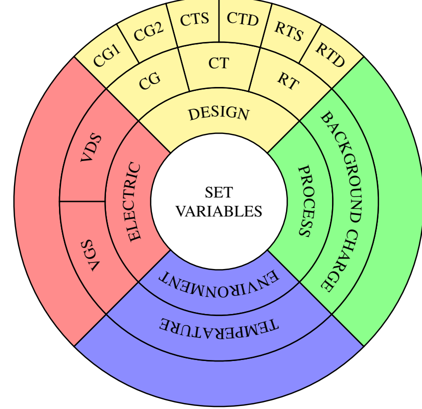


Fig. 2: SET variables that account for process, design, electric and environment.

3) Device-level simulation: Using SIMON simulator, a device-level simulator, characterization of the SET is performed for applied gate voltage of $|V_{GS}| \geq 200$mV in steps of 5mV. The effect of V_{DS} on SET operation is also characterized for voltages between 5mV to 195mV in steps of 5mV. Temperature is kept constant at 30K. The total capacitance of the island, C_Σ, is varied from 3aF to 4.5aF in steps of 0.5aF.

4) Expression generation: According to (4), each parameter of a sinusoidal function is computed. The amplitude and the frequency parameters are defined by the difference between, respectively, adjacent *y maxima* (or *y minima*) and two adjacent *x maxima* (or *x minima*) values for each I_D-V_{GS} curve. The amplitude and displacement are determined for each C_Σ and the results are shown in Figs. 3(a) and 3(b). Therefore, these are incorporated into the electrical model of the SET.

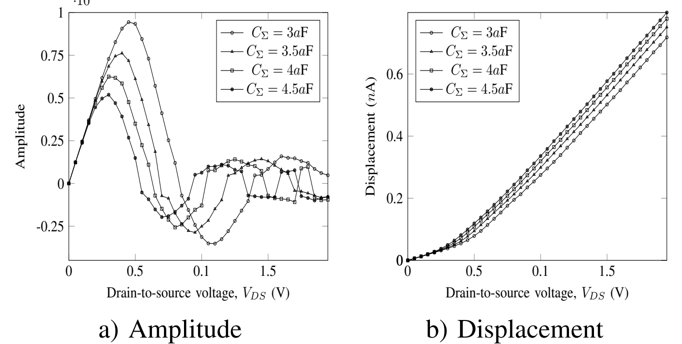


Fig. 3: Calculation of the amplitude and the displacement parameters as a function of V_{DS} for C_Σ values of 3aF, 3.5aF, 4aF, and 4.5aF.

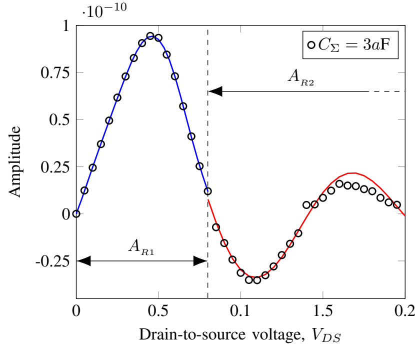


Fig. 4: Analysis of the amplitude parameter A in (4).

Analytical expressions are found in [7], [8] for the SET, which are incorporated in the proposed model through the relation $V_{DS} \propto \lambda e/C_\Sigma$, where λ is a real number. In addition, for $V_{DS} > 3e/C_\Sigma$ the Coulomb Blockade is negligible [2]. As a result, the SET begins to display a quasi-linear behavior similar to a two-terminal resistor. Therefore, the amplitude parameter is defined by two regions of operation as shown in Fig. 4, which are given as

$$A_{R1} = \sum_{n=1}^{7} k_n V_{DS}^n, \text{ and} \tag{5}$$

$$A_{R2} = k_7 \left(\frac{\sin(k_8 V_{DS} - 1)}{k_8 V_{DS} - 1} - \frac{\sin(k_8 V_{DS} + 1)}{k_8 V_{DS} + 1} \right). \tag{6}$$

where the k coefficients are computed for each A-V_{DS} curve. After applying a curve-fitting technique, the resulting numerical values are provided in Table I [9]. As a consequence, A_{R1} and A_{R2} are functions of V_{DS}.

In order to incorporate the C_Σ variable into the model, a polynomial representation for each column of Table I [9] is computed. The set of polynomial fitting parameters are described by (1) in [9]. After determining the polynomials, (5) and (6) are now functions of both V_{DS} and C_Σ.

A piece-wise exponential technique is applied to combine the A_{R1} and A_{R2} regions, as given by (7). The hyperplanes include an exponential term.

$$A(V_{DS}, C_\Sigma) = \frac{A_{R1}(V_{DS}, C_\Sigma)}{1 + e^{300V_{DS} - 24.135}} + \frac{A_{R2}(V_{DS}, C_\Sigma)}{\frac{1}{e^{300V_{DS} - 24.135}}}. \tag{7}$$

An approach similar to the characterization of the amplitude parameter is completed to determine the displacement parameter. For the displacement parameter, however, the SET is divided into three operating regions (D_{R1}, D_{R2}, and D_{R3}) as shown in Fig. 5, which are given as

$$D_{R1} = \sum_{n=1}^{5} k_n V_{DS}^n \tag{8}$$

$$D_{R2} = \sum_{n=6}^{8} k_n V_{DS}^n \tag{9}$$

$$D_{R3} = \frac{\left(V_{DS} - \frac{e}{C_\Sigma}\right)}{R_{TS} + R_{TD}} \tag{10}$$

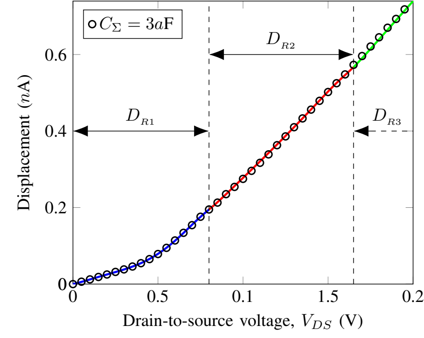


Fig. 5: Analysis of the displacement parameter, which has been curve-fitted across all operation regions of the SET transistor.

The displacement parameter includes eight coefficients ($k_{[1-8]}$) that are included in (8), (9), and (10). The corresponding computed value for each coefficient is listed in Table II [9] for C_Σ values of 3aF, 3.5aF, 4aF, and 4.5aF.

The set of polynomials computed to include C_Σ within the displacement parameter is given by (2) [9]. The overall shape of the displacement parameter is described by (11), where a piece-wise technique is also used to generate a single equation.

$$D(V_{DS}, C_\Sigma) = \frac{D_{R1}}{1 + e^{300V_{DS} - 24.135}} + D_{R2}\left(\frac{1}{e^{300V_{DS} - 48.27}} - \frac{1}{e^{300V_{DS} - 24.135}} \right) + \frac{D_{R3}}{1 + e^{300V_{DS} - 48.27}}. \tag{11}$$

The warping function developed for the SET model is expressed as

$$\frac{\mathrm{e}^{b(1/2\,\cos(x) + 1/2)} - 1}{\mathrm{e}^{b} - 1} - 1/2, \tag{12}$$

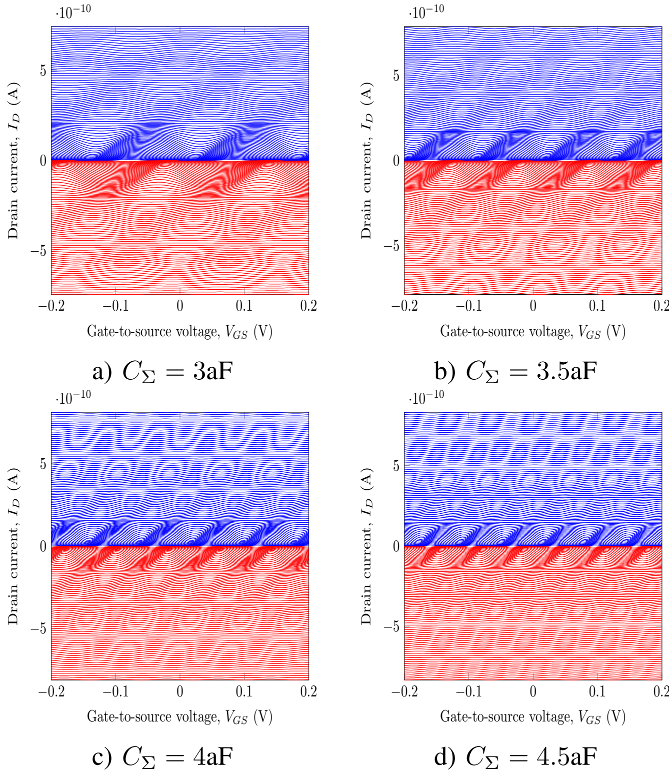
where x represents the frequency and the phase, which are given by (1) and (2), respectively. Note that (12) has a single fitting coefficient b, which is defined as

$$b = \frac{1.2\, e \sin\left(1.5\, \frac{\pi\, C_\Sigma\, V_{DS}}{e}\right)}{C_\Sigma\, V_{DS}}, \tag{13}$$

where e is the elementary charge.

The evaluation of the model is shown in Fig. 6. The Coulomb Blockade is visible in the figure, which is a characteristic of SET devices.

5) SET functional model: The resulting analytical equation of the SET is coded as a module in a hardware description language (HDL). The module can be incorporated as user-defined model that is invoked as a sub-circuit in a SPICE-like simulator.



a) $C_\Sigma = 3$aF b) $C_\Sigma = 3.5$aF

c) $C_\Sigma = 4$aF d) $C_\Sigma = 4.5$aF

Fig. 6: Evaluation of the (4) for positive and negative values of V_{DS} as a function of C_Σ.

IV. Simulation results using the SET model

In order to verify the performance of the model, two versions of inverter circuits are implemented. The first inverter is composed of two SETs [10], as shown in Fig. 7(a). In this case, R_{TD} and R_{TS} are set to 100MΩ. The second inverter consists of a PMOS transistor as a load and a SET as a driver [11]-[12], as shown in Fig. 7(b). For this case, $C_\Sigma = 3$aF and $W/L = 260\text{nm}/130\text{nm}$. The V_{in} and V_{out} characteristics of both topologies is shown in Figs. 8(a) and 8(b), respectively, where a comparison between the model proposed (plus signs) and a ME model [2] (circles) is used to verify accuracy. The VERILOG-A module used for the simulation is available upon request. Both inverters are simulated at a temperature of 30K with a $q_{BC} = 0$.

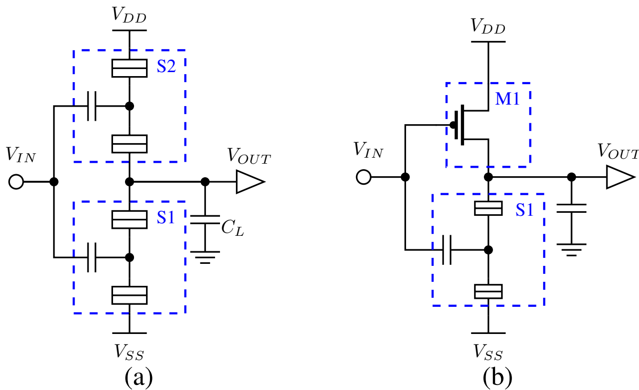
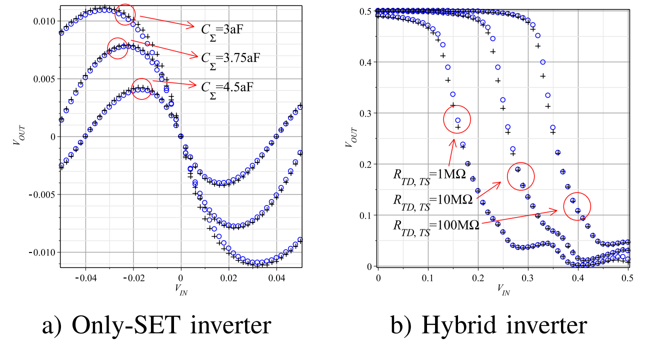


Fig. 7: Schematic of inverters, a) SET-only and b) hybrid CMOS/SET inverter.



a) Only-SET inverter b) Hybrid inverter

Fig. 8: DC analysis of a) SET-only inverter and b) hybrid inverter.

V. Conclusions

A SET behavioral model has been developed in a semi-symbolic form. The model is used for the electric simulation of both SET-only and hybrid circuits containing single-electron and MOS transistors through a VERILOG-A equivalent model that is used in a SPICE-like circuit simulator. The simulation results, when compared to the ME approach model, show agreement. As a result, the simulation methodology accurately simulated the electrical behavior of SET/MOS circuits.

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