Bi-directional Input/Output Circuits with Integrated Level Shifters for Near-threshold Computing

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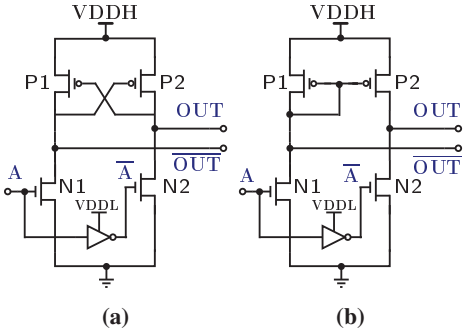
***Abstract*—Interfacing techniques for near-threshold computing are described in this paper. A bi-directional input/output circuit with integrated level shifters is proposed for multiple near-threshold power domains. The circuit provides conversion ranges of 0.38 V to 1.2 V and 0.45 V to 3.3 V depending on the targeted output voltage. Eight different configurations of I/O circuits are evaluated with level shifters implemented with a standard current mirror, cross coupled, and the proposed single ended topology. The use of a single ended level shifter provides the optimum power-delay point. The I/O circuit, at a core voltage of 0.45 V, consumes 4.87 mW with a fanout of four (FO4) delay of 0.46 for a V_{DOUT} and V_{PAD} voltage of, respectively, 0.45 V and 3.3 V. For a $V_{DD,L}$ of 0.625 V and $V_{DD,H}$ of 1.5 V, the delay and total power consumption of the single ended level shifter are, respectively, 0.74x and 0.4x that of a current mirror level shifter.**

I. Introduction

Near-threshold computing (NTC), where the supply voltage is set close to the threshold voltage of the transistor, is an effective method for ultra low power computation. The optimal power-performance point is achieved at a near-threshold supply voltage, which varies across logic, memory, input/output, and peripheral analog and mixed-signal circuit blocks [1]. In addition, systems on chip (SoC) and multi-core systems contain multiple power domains for improved energy efficiency while meeting targetted performance requirements [1]. Novel interface circuits are, therefore, required when data is transferred between near-threshold circuits and circuits operating on a separate power domain as interfacing techniques designed for nominal voltage operation are not optimal at near-threshold.

Techniques to interface between voltage domains of an IC implement either input/output (I/O) circuits or level shifters. The primary advantages of a bidirectional I/O circuit over a level shifter are the inclusion of an input receiver mode and a tristate output driver mode. Prior work on bidirectional I/O circuits examined the interface between a nominal supply voltage for the IC and a separate I/O voltage with integrated level shifters [2], [3]. However, the interface (I/O circuit) between near- and nominal-threshold circuits is rarely addressed.

Bidirectional I/O circuits with integrated level shifters are proposed in prior work for nominal supply voltages, where cross coupled level shifters are used for low power consumption [2], [3]. However, cross coupled level shifters are not optimal when supply voltages are set close to or below the transistor threshold voltage. For example, minimum input voltages of 0.55 V and 0.625 V are required to up-convert to output voltages of, respectively, 1.2 V and 3.3 V. In addition, the overall delay and power consumption of an I/O circuit increases for a longer level shifter delay. In this paper, a novel bidirectional I/O circuit that implements a combination of integrated level shifters is proposed. In addition, standard implementations of the level shifters are evaluated for comparison with the proposed configurations of the I/O circuit. Prior work has explored level shifter topologies for ultra low power and low voltage operation. Level shifters based on two types of circuit topologies; 1) cross-coupled [4], and 2) current mirror [5], are implemented as shown in Fig. 1. At a near-threshold supply voltage, the primary drawbacks of cross coupled based level shifters are: 1) a very weak pull down network, even if the NMOS transistors are significantly larger than the PMOS transistors, 2) the inability to change the set values at the outputs OUT and $\overline{OUT}$ as the NMOS transistors do not drain enough current to overcome the supplied current from the pull-up keeper at the lower supply voltages, and 3) increased delay. The primary drawback of current mirror based level shifters is an increased power consumption due to a static current path. In this work, a single ended level shifter is proposed to mitigate the drawbacks of conventional cross coupled and current mirror level shifters. The primary contributions of the paper are: 1) a single ended level shifter, and 2) a bidirectional I/O circuit with integrated level shifters optimized for interfacing with near-threshold circuits.



(a) **(b)**

Fig. 1: Conventional level shifter topologies. a) Cross coupled, and b) current mirror.

II. Single ended level shifter for NTC

A single ended input topology of the level shifter is proposed for near-threshold operation. The proposed level shifter is shown in Fig. 2, where input A operates at a near-threshold supply voltage. The single ended level shifter is compared with standard implementations of the cross coupled and current mirror based level shifters. A comparison of the conversion range, total power consumption, and propagation delay is performed. In addition, the proposed level shifter is compared with state-of-the-art low voltage level shifters. The operation of the single ended level shifter is as follows: Assume a nominal voltage of $V_{DD,H}$ and near-threshold voltage of $V_{DD,L}$, each set to, respectively, 1.2 V and 0.45 V. For an applied input of 0.45 V on N1, the $\overline{OUT}$ node discharges through N1 and N2 turns off, which results in a logic high at the OUT node.

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Note that a higher resistive path is required through N2 as compared to N1 to minimize charge leakage at OUT while $\overline{OUT}$ is transitioning to logic low. In addition, for an applied input of 0 V at the gate of N1, a nominal supply voltage of 1.2 V is applied to the gate of N2. The OUT node, therefore, discharges faster than $\overline{OUT}$, which reduces the propagation delay at a cost of increased power consumption. Note that for a set $V_{DD,H}$ of 1.2 V, $\overline{OUT}$ discharges to a minimum voltage level of 80 mV and 312 mV for a $V_{DD,L}$ of, respectively, 0.45 V and 0.4 V as there is a direct path from $V_{DD,H}$ to ground through P1 and N1. For input voltages below 0.4 V, the single ended level shifter does not operate as intended, since the voltage on $\overline{OUT}$ exceeds the threshold voltage of N2 (when 0 V is expected). Applying a voltage comparable to the threshold voltage of transistor N1 is sufficient to change the voltage at OUT, which results in an increased conversion range for the single ended level shifter as compared to the cross-coupled level shifter. The circuit techniques for improved energy efficiency implemented for cross coupled and current mirror based level shifters such as the use of a revised wilson current mirror [5] or a split input inverting buffer [4] also apply to the single ended level shifter.

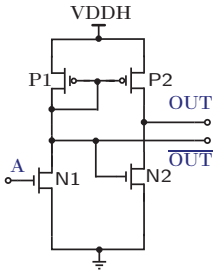


Fig. 2: Proposed level shifter with single ended input and differential output.

III. Bi-directional input/output circuits

The proposed bi-directional I/O circuit for near-threshold operation is shown in Fig. 3, where integrated level shifters are labeled as *Level Shifter 1 (LS1)* and *Level Shifter 2 (LS2)*. The application of the near-threshold voltage CVDD to the core and the nominal or I/O voltage NVDD are also shown in Fig. 3. The control signals IN_IDLE and EN set the operation of the I/O circuit to, respectively, input and output mode. For example, a logic high EN signal forces the outputs of the NAND1 and NOR to, respectively, logic high and logic low. The output driver, therefore, remains in a high impedance state. In addition, a logic low at the NAND2 gate forces the inputs DIN1 and DIN2 to logic low, irrespective of the signal on the PAD terminal. Additional level restorers are implemented using PMOS transistors P2 and P3 to prevent an unwanted switching at the input terminals DIN1 and DIN2 of the core.

Depending on the specific application, the optimum power-performance point requires multiple near-threshold power domains with a difference of tens of millivolts. Therefore, multiple input buffers (DIN1 and DIN2) are proposed within a single I/O circuit, where the implemented power domains are labeled as CVDD1 (0.4 V) and CVDD2 (0.45 V). The properties of the proposed I/O circuit are: 1) an optimized level shifter topology, where a fast conversion rate is required for *LS1* and an energy efficient topology is required for *LS2*, 2) isolation of the input circuits from the transients of the external signals by implementing level restorers P2 and P3 and applying IN_IDLE on NAND2, which reduce both the noise and power consumption, and 3) multiple near-threshold input modes for fine grain energy-efficiency in an integrated circuit with multiple voltage domains.

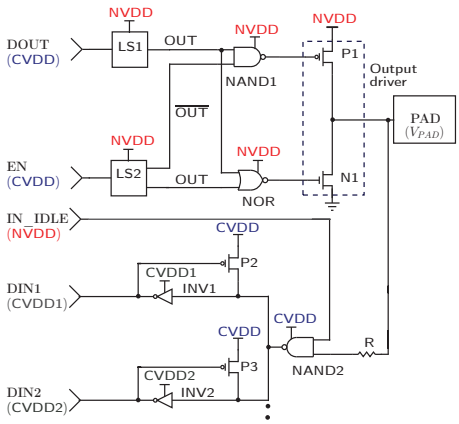


Fig. 3: Proposed bidirectional input/output circuit.

IV. Simulated Results of Interface Circuit

Characterization of the interface circuit is described in this section. The simulation setup is provided in Section IV-A. The level shifters and I/O circuits are characterized in Sections IV-B and IV-C, respectively.

A. Simulation setup

The simulation of the level shifters and I/O circuits is performed using an IBM 130 nm technology. The area of both the cross coupled and current mirror level shifters is 3.64 μm^2, while the area of the single ended level shifter is 2.47 μm^2 (calculated from the listed transistor sizes in Table I). The level shifters and I/O circuits are simulated at, respectively, 17 MHz and 100 MHz operating frequencies. An output load of 5 fF is used for all data paths, which is more than 10x larger than the calculated gate capacitance of a standard CMOS inverter in the 130 nm technology node. The low to high voltage level shifters are simulated for multiple input ($V_{DD,L}$) and output ($V_{DD,H}$) voltages for comparison of the conversion range, total power consumption, and propagation delay. The nominal core and I/O voltage levels are set to, respectively, 1.2 V and 3.3 V. Supply voltages of 0.4 V and 0.45 V are considered for near-threshold as the transistor threshold voltages range from 0.35 V to 0.42 V. The proposed I/O circuit is evaluated through eight different configurations using the current mirror, cross-coupled, and the proposed single ended level shifter, as listed in Table II. SPICE simulation to characterize the conversion range, total power, and propagation delay is performed for a set value of EN and IN_IDLE. EN is set to 0 V when the I/O circuit is in output mode, and IN_IDLE is set to 0 V when in input mode.

B. Characterization of level shifters

The conversion range of all level shifters is analyzed for output voltages of 1.2 V and 3.3 V. Note that the conversion

TABLE I: Transistor size of the level shifters.

Cross coupled	Current mirror	Single ended
P1, P2,= 2 µm/0.13 µm x 2 N1, N2 = 8 µm/0.13 µm x 2 PMOS (Inverter) = 6 µm/0.13 µm NMOS (Inverter) = 2 µm/0.13 µm		P1, P2 = 0.6 µm/0.13 µm x 2 N1 = 18 µm/0.13 µm N2 = 0.4 µm/0.13 µm

TABLE II: Configurations of the I/O circuits based on the type of implemented level shifters.

Configuration	Level shifter 1	Level shifter 2
A	cross coupled	cross coupled
B	cross coupled	current mirror
C	single ended	cross coupled
D	single ended	single ended
E	single ended	current mirror
F	current mirror	single ended
G	current mirror	current mirror
H	current mirror	cross coupled

range shifts with a change in the output voltage $V_{DD,H}$. The current mirror level shifter and single ended level shifter have an approximately equal conversion range of 0.4 V to 1.2 V and 0.5 V to 3.3 V for output voltages of, respectively, 1.2 V and 3.3 V. However, the cross coupled level shifter exhibits a reduced conversion range of 0.5 V to 1.2 V and 0.625 V to 3.3 V for output voltages of, respectively, 1.2 V and 3.3 V. The propagation delay of the level shifters is compared with an inverter FO4 delay over a range of input voltages $V_{DD,L}$ and for a set output voltage of 1.2 V, as shown in Fig. 4. The single ended level shifter exhibits the minimum delay for all values of $V_{DD,L}$. For example, for a set $V_{DD,L}$ of 0.55 V and $V_{DD,H}$ of 1.2 V, the propagation delay of a FO4 inverter (for process characterization), cross coupled level shifter, and current mirror level shifter is, respectively, 4.62x, 2.72x, and 1.42x longer than the single ended level shifter.

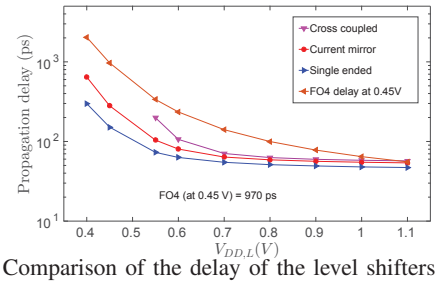
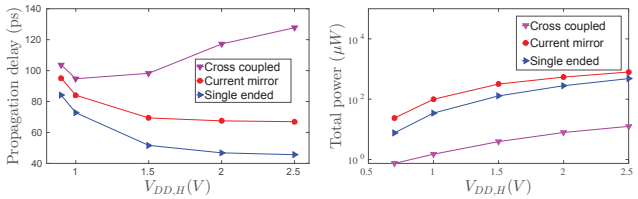


Fig. 4: Comparison of the delay of the level shifters at an output voltage $V_{DD,H}$ of 1.2 V.

The comparison of the propagation delay and total power consumption of the level shifters is performed for a set $V_{DD,L}$ of 0.625 V as $V_{DD,H}$ is swept from 0.7 V to 3.3 V. The delay of the cross coupled level shifter increases with increasing output voltage, while the delay of the current mirror and single ended level shifters is reduced for higher output voltages, which is shown in Fig. 5(a). The reduction in delay is more significant at higher output voltages for the single ended level shifter as compared to the current mirror topology since a higher potential is applied to the gate of N2. The cross coupled level shifter consumes the least power of all topologies over the range of output voltages examined, as shown in Fig. 5(b). The power consumption of the single ended level shifter is, however, less than the current mirror topology over the entire range of output voltages. For a $V_{DD,L}$ of 0.625 V and $V_{DD,H}$ of 1.5 V, the propagation delay of the single ended level shifter is 0.53x and 0.74x the delay of, respectively, the cross coupled and current mirror level shifters. In addition, the total power consumption of the single ended level shifter is 33x and 0.4x the power consumed by, respectively, the cross coupled and current mirror level shifters. Although the cross coupled level shifter consumes much less power, the delay is significantly larger (4.62x) than the proposed single ended topology.



(a) **(b)**

Fig. 5: Comparison of the a) propagation delay, and b) total power of the level shifters for an input voltage $V_{DD,L}$ of 0.625 V.

The single ended level shifter exhibits reduced conversion delay with a significant power overhead as compared to the cross coupled level shifter, while exhibiting reduced delay and power consumption as compared to the current mirror level shifter. In addition, the cross coupled level shifter suffers from a fundamental limitation in the minimum voltage that can be converted for a given output voltage, where, for the 130 nm process, input voltages of 0.55 V and 0.625 V are required for output voltages of, respectively, 1.2 V and 3.3 V. The cross coupled level shifters are, however, beneficial for relatively large input voltages, where the propagation delay is not significantly impacted. A single ended level shifter therefore exhibits the best characteristics when operating at near-threshold voltages, as 0.4 V and 0.45 V are up-converted to, respectively, a nominal IC voltage of 1.2 V and an I/O voltage of 3.3 V with a faster conversion time as compared to cross coupled and current mirror topologies.

The conversion range, performance, energy per transition, and area of proposed level shifters are compared with state-of-the-art level shifters for near/sub-threshold operation, as listed in Table III. The proposed level shifter exhibits the smallest delay among the compared level shifter topologies, which is 0.146 FO4 delay (0.2986 ns) when converting from 0.4 V to 1.2 V. The energy overhead of the proposed level shifter is compensated by the energy savings in the I/O circuit, where short circuit power is significantly reduced due to the faster response time of *Level Shifter 1 (LS1)*.

C. Characterization of I/O circuit configurations

The conversion range of each type of I/O circuit configuration is listed in Table IV for PAD voltages V_{PAD} of 1.2 V and 3.3 V. Configurations *A* and *B* of the I/O circuit exhibit a limited conversion range for both PAD voltages since the cross coupled level shifters are used for *LS1* in Fig. 3. A comparison of the propagation delay and total power consumption of the different I/O circuit configurations is shown in, respectively, Fig. 6(a) and 6(b) across a range of V_{PAD} voltages and for a DOUT voltage V_{DOUT} of 0.55 V. Configurations *E* and *F* are implemented with, respectively, a

TABLE III: Comparison with state-of-the-art low voltage level shifters.

Parameters	VLSIC 2011** [6]	JSSC 2012* [7]	TCASI 2015** [5]	TCASI 2017* [8]	JLPEA 2016** [9]	TCASII 2017** [4]	This work *
Process	130 nm	350 nm	180 nm	180 nm	130 nm	180 nm	130 nm
Conversion range	0.3 V to 2.5 V	0.23 V to 3 V	0.21 V to 3.3 V	0.3 V to 1.8 V	0.145 V to 1.2 V	0.1 V to 1.8 V	0.4 V to 1.2 V, 0.5 V to 3.3 V
Delay (FO4)	2.38 (0.3 V to 2.5 V)	Not provided	≈1.05 (0.3 V to 1.2 V)	Not provided	Not provided	2.2 (0.3 V to 1.2 V)	0.146 (0.4 V to 1.2 V)
Delay (ns)	41.51 (0.3 V to 2.5 V)	≈8500 (0.4 V to 1.2 V)	≈170 (0.3 V to 1.2 V)	17.3 (0.4 V to 1.8 V)	>200	31.7 (0.4 V to 1.8 V)	0.2986 (0.4 V to 1.2 V)
Area (μm^2)	102.6	1880 **	153.01	229.5 **	466	108.8	2.47^
Energy/transition (fJ)	229 (0.3 V to 2.5 V)	≈4250 (0.4 V to 1.2 V)	≈8 (0.3 V to 1.2 V)	56 (0.4 V to 1.8 V)	1200 (0.145 V to 1.2 V)	173 (0.4 V to 1.8 V)	570 (0.4 V to 1 V), 1600 (0.45 V to 1.2 V)

* Simulated ** Measured ^Active channel area Note: FO4 delays are measured at VDDL

TABLE IV: Conversion range of I/O circuit configurations for V_{PAD} of 1.2 V and 3.3 V.

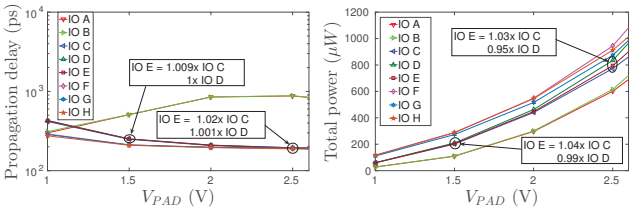
V_{PAD}	A, B	C, D, E, F, G, H
1.2 V	0.53 V to 1.2 V	0.38 V to 1.2 V
3.3 V	0.55 V to 3.3 V	0.45 V to 3.3 V

single ended and current mirror level shifter for *LS1*. Although there is only a minor increase in the propagation delay of the current mirror level shifter as compared to the single ended topology, the overall power consumption of the I/O circuit (configuration *F*) increases significantly with the use of a current mirror level shifter, where configurations *G* and *H* also exhibit similar characteristics. The power consumption of the pre-driver NAND1 and NOR gates increases significantly for a larger rise or fall time of the inputs due to increased short circuit current, which negatively impacts the overall power consumption of the I/O circuit. However, a set value of EN is used in this work, which avoids the periodic switching of the NOR gate. Configurations *A* and *B* exhibit the minimum power consumption with a significant increase in delay. However, *A* and *B* are not feasible for near-threshold operation unless the input voltage V_{DOUT} to *LS1* is at least 0.625 V.

Among the eight configurations, *C*, *D*, and *E* provide the optimum power-delay points as shown in Fig. 6, where the single ended level shifter is used in place of *LS1*. An improvement in the delay and power is seen for configuration *C* as compared to *D* and *E* for both a V_{PAD} of 1.5 V and 2.5 V (simulation was performed sweeping V_{PAD} from 0.7 V to 3.3 V), since the low power cross coupled level shifter is used in place of *LS2*. However, the use of the cross coupled level shifter limits the operating range of the I/O circuit. In addition, *D* and *E* exhibit almost similar power and delay results for both V_{PAD} voltages of 1.5 V and 2.5 V since *LS2* is not switching (EN is set to 0). Note that *E* is not affected by the increased delay of *LS2* as compared to *LS1*, since the switching frequency of the control signal EN is less likely to change than V_{DOUT}. Therefore, the use of a single ended level shifter in place of *LS1* and either a single ended or current mirror level shifter in place of *LS2* provides the optimum power-delay operating point with the maximum conversion range. The optimal configuration, *E*, at a supply voltage of 0.45 V (CVDD), consumes a total power of 4.87 mW and has a FO4 delay of 0.46 for a V_{PAD} voltage of 3.3 V.

V. Conclusions

In this paper, a single ended level shifter and bi-directional I/O circuit are proposed for near-threshold computing. The optimized configuration of the I/O circuit provides a conversion range of 0.38 V to 1.2 V for core voltages and 0.45 V to 3.3 V for I/O voltages. The use of a single ended level shifter provides the optimum power-delay point,



(a) **(b)**

Fig. 6: Comparison of different I/O circuit configurations for a V_{DOUT} of 0.55 V. a) Propagation delay, and b) total power consumption.

where configuration E consumes 4.87 mW of power with a 0.46 FO4 delay. In addition, the proposed circuit includes multiple near-threshold input buffers to provide conversion to the corresponding optimal core voltages. The single ended level shifter exhibits delays of 0.53x and 0.74x and power consumption of 33x and 0.4x as compared to, respectively, a cross coupled and current mirror level shifter. In addition, the single ended level shifter provides conversion ranges of 0.4 V to 1.2 V and 0.5 V to 3.3 V. The proposed I/O circuit and level shifter are, therefore, optimal to interface between near-threshold and the nominal core and I/O voltage domains.

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