Noise Constrained Optimum Selection of Supply Voltage for IoT Applications

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***Abstract*—An optimization technique is proposed to set the supply voltage of an integrated circuit for a given range of threshold voltages. The algorithm accounts for the variations in maximum operating frequency f_{max}, noise margins, and threshold voltage. The algorithmically determined supply and threshold voltages are compared with SPICE simulation for a 130 nm CMOS technology, where per cent error of up to 14% and 8% are observed for, respectively, the average noise margins NM_{avg} and f_{max} as compared to target circuit specifications for noise margin and frequency. The evaluated ranges of the supply and threshold voltages are, respectively, 200 mV $\leq V_{dd} \leq$ 1200 mV and 250 mV $\leq V_t \leq$ 700 mV. The technique is applied to both a 130 nm and 45 nm CMOS technology and results of noise margin and frequency are compared through SPICE simulation. The 45 nm technology node exhibits variation of up to 0.89× and 4.3× in, respectively, NM_{avg} and f_{max} as compared to an inverter in a 130 nm technology.**

I. Introduction

Energy efficiency and ultra-low power consumption have become the key drivers for many ultra-low power IoT applications. For a given technology and performance requirement, energy efficiency is determined by the appropriate selection of supply and threshold voltages. Supply voltage scaling provides an optimum power-delay and a minimum energy point at the expense of performance, while threshold voltage scaling improves the performance at the expense of reduced noise margins [1]–[5]. Prior research addressed supply and threshold voltage tuning considering switching speed, power consumption, total energy, and circuit characteristics [6]–[9]. However, the noise margins and f_{max} are rarely considered when optimizing the supply and threshold voltages. Aggressive supply voltage scaling in the range of the near- and sub-threshold voltage of a transistor severely degrades the noise margins and stability of the circuit [1], [10]. Threshold voltage scaling and deviation due to process, voltage, and temperature (PVT) variation reduce the robustness of the circuit to noise [1], [5], [10]. In addition, dynamic voltage and frequency scaling (DVFS) does not account for the noise margins of the circuit when the supply voltage is scaled to reduce the operating frequency of the circuit [11].

An exponential relationship exists between the supply voltage and the f_{max} of the circuit in sub-threshold (0.1 V to 0.4 V), as shown in Fig. 1. The NM_{avg} (mean of noise margins high and low) decrease linearly with supply voltage scaling, which is also shown in Fig. 1. In addition, variation in threshold voltage inversely affects the noise margins and f_{max}, as shown in Fig. 2. Therefore, an optimization of the supply and threshold voltages is required for different circuit constraints as there are trade-offs between operating frequency, energy efficiency, and robustness to noise.

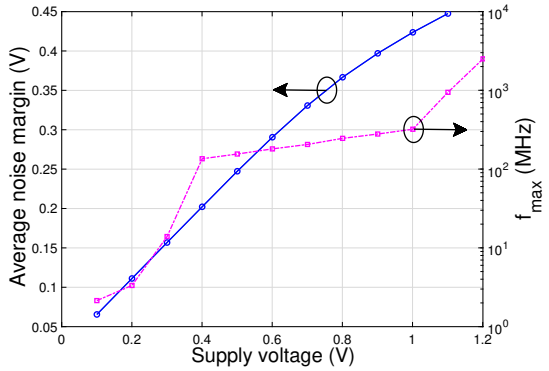

Fig. 1: Effects of supply voltage scaling for a 130 nm technology on f_{max} and NM_{avg} for a CMOS inverter with PMOS width W_p of 5.77 µm and NMOS width W_n of 2 µm.

In this paper, an optimization technique for selection of supply voltage is proposed for a given minimum and maximum range of threshold voltages. The optimization model is developed based on the variations in noise margins and f_{max} due to supply and threshold voltage variations. The change in threshold voltage due to supply voltage variation is also considered in the proposed model. For a given f_{max} and NM_{avg}, the proposed algorithm implicitly improves the energy-efficiency of the circuit by reducing the supply and threshold voltages. The rest of the paper is organized as follows: The description and evaluation of the proposed algorithm for the optimum selection of supply voltage is discussed in Section II. The simulation results are described in Section III. Concluding remarks are provided in Section IV.

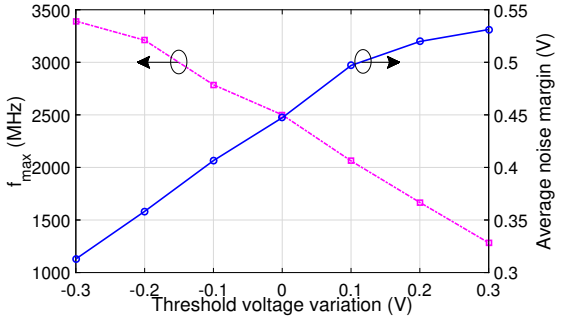

Fig. 2: Variation in the zero-bias threshold voltage of a CMOS inverter for a set supply voltage of 1.2 V.

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II. Selection of Optimum Supply and Threshold Voltage

The procedure to optimize the supply and threshold voltages of an inverter is described by Algorithm 1. The problem formulation and description of the parameters required for the algorithm are provided in Section II-A. The expansion of the algorithm for more complex circuits that include a larger number of gates is described in Section II-B.

A. Problem Formulation

The operating characteristics of an integrated circuit are affected by changes in the supply and threshold voltages. A reduction in supply voltage reduces both the noise margins and the f_{max}. However, a reduction in threshold voltage reduces the noise margins, but increases the f_{max}. The changes in the operating characteristics of the circuit due to variation in supply and threshold voltage are accounted for by the proposed optimization model described in this paper. Note that the supply voltage, threshold voltage, noise margin, and operating frequency are all of different units. Therefore, a common unitless representation of all variables is considered for the optimization model. One unit of supply voltage (or threshold voltage or noise margin) and one unit of operating frequency are set to, respectively, 100 mV and 100 MHz. In addition, the parameters implemented in the algorithm are considered based on a single CMOS inverter.

Algorithm 1 Supply and Threshold Voltage Optimization

$$\begin{aligned}
&\min && x \cdot NPP_{Vdd} + y \cdot NPP_{Vt} \\
&\text{s.t.} && N_{Vdd} \cdot x + N_{Vt} \cdot y \geq N_m \\
& && P_{Vdd} \cdot x - P_{Vt} \cdot y \geq P_m \\
& && V_{t,min} = V_{t,min} + \Gamma \cdot V_{dd,min} \\
& && V_{dd,max} \geq x \geq V_{dd,min} \\
& && V_{t,max} \geq y \geq V_{t,min} \\
& && x, y \geq 0
\end{aligned}$$

where,

- x = number of units of supply voltage,
- y = number of units of threshold voltage,
- N_m = minimum required noise margin,
- P_m = minimum required operating frequency,
- $V_{dd,min}$ and $V_{dd,max}$ = minimum and maximum allowed supply voltage,
- $V_{t,min}$ and $V_{t,max}$ = minimum and maximum allowed threshold voltage, and
- Γ = fitting parameter that accounts for the change in threshold voltage for variation in supply voltage

1) Definition 1 - NPP: A design metric is introduced to optimize the supply voltage algorithmically, which is described as the noise performance product (NPP). The NPP is the product of the NM_{avg} and the f_{max}. The change (reduction or increase) in the noise performance product as the supply and threshold voltages are modified is given by, respectively, NPP_{Vdd} and NPP_{Vt}. For a given technology and supply voltage, a higher value of NPP is desired to meet the noise constraints and frequency requirements of the circuit.

2) Definition 2 - N_{Vdd}: A change (reduction or increase) in NM_{avg} for each unit of scaling of the supply voltage V_{dd}, where smaller noise margins are expected at lower V_{dd}. For example, an N_{Vdd} of 0.5 implies the NM_{avg} is reduced by 50 mV when the supply voltage is reduced by 100 mV.

3) Definition 3 - N_{Vt}: A change in NM_{avg} for each unit of scaling of the threshold voltage V_t, where a reduction is expected with lower V_t.

4) Definition 4 - P_{Vdd}: A change in the f_{max} for each unit of scaling of the supply voltage V_{dd}, where a reduction is expected at lower V_{dd}. For example, a P_{Vdd} of 0.5 implies the maximum operating frequency is reduced by 50 MHz when the supply voltage is scaled by 100 mV.

5) Definition 5 - P_{Vt}: A change in f_{max} for each unit of scaling of the threshold voltage V_t, where an increase is expected for lower V_t.

The objective function accounts for the reduction in the noise performance product due to the scaling of the supply and threshold voltages. The first constraint limits the NM_{avg} to at least equal or greater than N_m, while subject to the reduction in noise margins due to supply and threshold voltage scaling. The algorithm will, therefore, not return any determined supply and threshold voltage values that result in an NM_{avg} that is less than the minimum required noise margin for the circuit. The second constraint limits the f_{max} to at least equal or greater than P_m, while subject to a reduction in operating frequency due to supply voltage scaling. Note that a negative value for P_{Vt} is assumed since f_{max} increases as the threshold voltage is reduced. The third and fourth constraint define the ranges of, respectively, supply and threshold voltage. Note that the minimum and maximum values of allowed supply and threshold voltages are determined based on the implemented fabrication technology and application. The reduction in supply and threshold voltages reduce the value of, respectively, NPP_{Vdd} and NPP_{Vt}. The algorithm minimizes the reduction in the NPP metric and provides the optimum supply voltage for a target operating frequency and noise margin for a target range of threshold voltages. In addition, the change in the threshold voltage due to variation in the supply voltage is also included in the model.

B. Expansion of the algorithm for larger circuit blocks

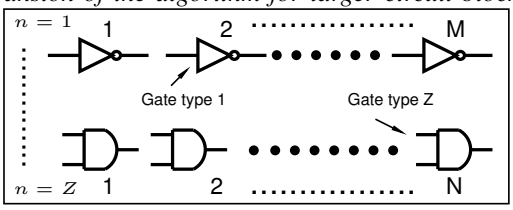

Fig. 3: Expanding Algorithm 1 for multi-gate circuits.

The algorithm is applied to a circuit block with a large number of gates as shown in Fig.3. There are a total of M and N number of, respectively, NOT and AND gates in the circuit. Note that only two types of gates are implemented in this particular circuit block. The objective function is rewritten for the two types of gates as given by (1), where the first constraint

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for noise margins (N_{Vdd} and N_{Vt}) and the second constraint for maximum frequency (P_{Vdd} and P_{Vt}) are modified.

$$\begin{aligned}\min \quad & x \cdot [NPP_{Vdd}(\text{NOT}) \cdot M + NPP_{Vdd}(\text{AND}) \cdot N] \\ & + y \cdot [NPP_{Vt}(\text{NOT}) \cdot M + NPP_{Vt}(\text{AND}) \cdot N] \qquad (1)\end{aligned}$$

s.t.

$$\begin{aligned}&[N_{Vdd}(\text{NOT}) \cdot M + N_{Vdd}(\text{AND}) \cdot N] \cdot x + [N_{Vt}(\text{NOT}) \cdot M + \\ &\quad N_{Vt}(\text{AND}) \cdot N] \cdot y \geq [N_m(\text{NOT}) \cdot M + N_m(\text{AND}) \cdot N] \\ &[P_{Vdd}(\text{NOT}) \cdot M + P_{Vdd}(\text{AND}) \cdot N] \cdot x - [P_{Vt}(\text{NOT}) \cdot M + \\ &\quad P_{Vt}(\text{AND}) \cdot N] \cdot y \geq [P_m(\text{NOT}) \cdot M + P_m(\text{AND}) \cdot N]\end{aligned}$$

The supply and threshold voltage selection procedure is also generalized for Z types of gate in a circuit as described by Algorithm 2, where the number of gate types n ranges from 1 to Z. Note that an equal N number of gates for each type of logic is assumed. In addition, a similar supply voltage is assumed for all gates, and a similar threshold voltage is assumed for all transistors.

Algorithm 2 Modification of Algorithm 1 for multi-gate circuits

$$\begin{aligned}\min \quad & x \cdot \sum_{n=1}^{Z} NPP_{Vdd}(n) \cdot N(n) + y \cdot \sum_{n=1}^{Z} NPP_{Vt}(n) \cdot N(n) \\ \text{s.t.} \quad & x \cdot \sum_{n=1}^{Z} N_{Vdd} \cdot N(n) + y \cdot \sum_{n=1}^{Z} N_{Vt} \cdot N(n) \geq \sum_{n=1}^{Z} N_m \cdot N(n) \\ & x \cdot \sum_{n=1}^{Z} P_{Vdd} \cdot N(n) - y \cdot \sum_{n=1}^{Z} P_{Vt} \cdot N(n) \geq \sum_{n=1}^{Z} P_m \cdot N(n) \\ & V_{t,min} = V_{t,min} + \Gamma \cdot V_{dd,min} \\ & V_{dd,max} \geq x \geq V_{dd,min} \\ & V_{t,max} \geq y \geq V_{t,min} \\ & x, y \geq 0\end{aligned}$$

III. Simulation Results and Analysis

A. Method of Evaluation

The proposed algorithm is evaluated using SPICE simulation in both a 130 nm and 45 nm technology node. The parameters determined through execution of Algorithm 1 for a 130 nm technology are used in simulation to compare NM_{avg} and f_{max} for both a 130 nm and 45 nm technology to analyze the effect of scaling on voltage selection. The supply and threshold voltages for both nodes are optimized by Algorithm 1 for the target noise margins and frequencies listed in Table I. The $V_{dd,min}$, $V_{dd,max}$, $V_{t,min}$, and $V_{t,max}$ are chosen approximately based on the minimum and maximum allowable voltages in a 130 nm technology. Note that without the application of body biasing, the range of threshold voltages in a 130 nm technology for PMOS and NMOS transistors is, respectively, $-0.3V \geq V_{t,p} \geq -0.435V$ and $0.45V \geq V_{t,n} \geq 0.35V$. The NM_{avg} and f_{max}, which are shown in Fig. 1, are used to calculate the noise performance product for the range of supply voltages between 0.2 V and 1.2 V. The average change in noise margins and f_{max} due to supply and threshold voltage variations is used to calculate the values of NPP_{Vdd}, NPP_{Vt}, N_{Vdd}, N_{vt}, P_{Vdd}, and P_{Vt}. The N_m and P_m are design and technology dependent parameters. Note that the use of the average value of P_{Vdd} reduces computational complexity at the cost of accuracy for the given range of supply voltages (0.2 V to 1.2 V), while the use of a smaller supply voltage range improves the accuracy (see f_{max} in Fig. 1).

B. Comparison of the algorithm with simulation results

The required parameters to evaluate the algorithm are extracted using SPICE simulation. The average variation in NPP_{Vdd} (NPP_{Vt}) for a reduction in V_{dd} (V_t) by one unit is 3.484 (1.02073). The reduction (increase) in P_{Vdd} (P_{Vt}) for scaling of V_{dd} (V_t) by one unit is 2.49667 (2.91767). The reduction in N_{Vdd} (N_{Vt}) for scaling of V_{dd} (V_t) by one unit is 0.23 (0.40). In addition, Γ is determined as 0.01862 by characterizing the change in threshold voltage for variation in supply voltage for the 130 nm technology. The parameters for the algorithm described in Section II are used to solve for x and y for the six different test cases listed in Table I, where the optimum supply voltage is obtained for a given maximum and minimum range of threshold voltages and for the required noise margins and operating frequency. A similar range of possible supply voltages (200 mV $\leq V_{dd} \leq$ 1200 mV) is used for all test cases, while different ranges of possible threshold voltages are used to determine the optimum supply and threshold voltages.

The optimum V_{dd} and V_t listed in Table I are used to determine the f_{max} and NM_{avg} through SPICE simulation, which are listed in Table II. The noise margins are determined using the voltage transfer curve of a CMOS inverter through SPICE simulation. Body biasing is used to tune the threshold voltages to the values obtained from execution of Algorithm 1. The noise margin and maximum frequency obtained from SPICE simulation are compared with the constraints used in Algorithm 1. The optimization of V_{dd} and V_t results in up to 14% error for the six test cases considered (see Tables I through III), while maintaining the NM_{avg} provided as a constraint, and exhibits an error from the targeted operating frequency of up to 8%.

Test Cases 2 and 6 have similar constraints, but with differences in the range of possible threshold voltages of, respectively, 400 mV $\leq V_t \leq$ 420 mV and 300 mV $\leq V_t \leq$ 700 mV. However, Test 2 requires a higher supply voltage as compared to Test 6, as the minimum threshold voltage for Test 2 is larger than the minimum threshold voltage for Test 6. In addition, despite the use of different supply and threshold voltages for Test 2 and 6, the SPICE simulation for each case remains within 0.86× to 1.13× and 1.05× to 1.08× (normalized to results from the model for each case) of, respectively, the expected NM_{avg} and expected f_{max}. A similar constraint for the noise margins is applied in Tests 1 and 5. However, a larger value for the performance constraint is applied in Test 1 as compared to Test 5, which results in a larger supply voltage for Test Case 1. Additionally, Tests 3 and 4 are constrained by similar values of operating frequency and threshold voltage. However, Test 4 provides a higher optimum voltage as compared to Test 3 due to an increased noise margin constraint.

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TABLE I: Optimization of V_{dd} and V_t for constraints N_m, P_m, V_{dd} range, and V_t range.

Test	N_m **(mV)**	P_m **(MHz)**	V_{dd} **range (mV)**	V_t **range (mV)**	**Optimum** V_{dd} **(mV)**	**Optimum** V_t **(mV)**
1	≥ 400	≥ 350	$200 \le V_{dd} \le 1200$	$350 \le V_t \le 420$	1009	420
2	≥ 190	≥ 150	$200 \le V_{dd} \le 1200$	$400 \le V_t \le 420$	527	406
3	≥ 350	≥ 250	$200 \le V_{dd} \le 1200$	$350 \le V_t \le 420$	791	420
4	≥ 370	≥ 250	$200 \le V_{dd} \le 1200$	$350 \le V_t \le 420$	878	420
5	≥ 400	≥ 300	$200 \le V_{dd} \le 1200$	$250 \le V_t \le 500$	870	500
6	≥ 190	≥ 150	$200 \le V_{dd} \le 1200$	$300 \le V_t \le 700$	418	306

TABLE II: Characterization of NM_{avg} and f_{max} through SPICE simulation with optimally selected V_{dd} and V_t.

Test	V_{dd} **(mV)**		V_t **(mV)**		NM_{avg} **(mV)**		f_{max} **(MHz)**		**% error** (NM_{avg})	**% error** (f_{max})
	Model	SPICE (applied)	Model	SPICE (applied)	Model	SPICE (determined)	Model	SPICE (determined)		
1	1009	1009	420	419.85	≥ 400	404.71	≥ 350	322	-1.178	8
2	527	527	406	406.05	≥ 190	214.8	≥ 150	162.4	-13.05	-8.267
3	791	791	420	420.9	≥ 350	328.66	≥ 250	245.7	6.09	1.72
4	878	878	420	421.8	≥ 370	362.38	≥ 250	260	2.06	-4
5	870	870	500	501.85	≥ 400	367.355	≥ 300	288	8.16	4
7	418	418	306	306.9	≥ 190	163.4	≥ 150	157.1	14	-4.73

The SPICE results obtained for a 130 nm technology node are compared with the SPICE results for a 45 nm technology, as listed in Table III. Note that similar supply voltage ranges are used in 45 nm, while the threshold voltages (-384 mV for PMOS and 410 mV for NMOS) are kept constant to characterize the difference in simulation results between 130 nm and 45 nm while controlling for changes to the threshold voltage due to increased sensitivity to PVT variation for scaled technologies [1], [5], [10].

The f_{max} increases when transistor gate length is reduced [12]. The propagation delay is given by (2). Assuming the transistor is in saturation, the delay is proportional to the square of the gate length. The μ and L in (2) are, respectively, the electron mobility and transistor gate length. Assuming a constant V_{dd}, V_t, and μ, the delay for a 130 nm technology is approximately 8.3× that of a 45 nm inverter. Therefore, the f_{max} in 45 nm is up to 4.3× greater than the maximum frequency of an inverter in 130 nm (for Test Case 4). However, the noise margin in 45 nm is reduced to 0.89× the noise margin of the 130 nm inverter (for Test Case 1).

$$\text{Propagation delay, } t_p \propto \frac{L^2 \times V_{dd}}{\mu(V_{dd} - V_t)^2} \tag{2}$$

TABLE III: Comparison of average noise margin and maximum frequency between 130 nm and 45 nm technologies.

Test	NM_{avg} **(mV)**			f_{max} **(MHz)**		
	Model (constraint)	130 nm (determined)	45 nm (determined)	Model (constraint)	130 nm (determined)	45 nm (determined)
1	≥ 400	404.712	359	≥ 350	322	1123.6
2	≥ 190	214.8	205.3	≥ 150	162.4	666.7
3	≥ 350	328.66	304	≥ 250	245.7	1010.1
4	≥ 370	362.38	329	≥ 250	260	1111
5	≥ 400	367.4	326.9	≥ 300	288	1091.7
6	≥ 190	163.4	158.7	≥ 150	157.1	621.1

C. Feasible region of the optimal solution

The feasible region and optimum solution for selection of the supply and threshold voltages are discussed in this section as a means to analyze the solution obtained from the algorithm. The feasible region and the contour plot representing different optimum solutions are shown in Fig. 4, where the constraints of Test Case 5 are used. The feasible region is bounded by the constraints for noise margins (0.23x + 0.4y = 4), supply voltage (200 mV ≤ V_{dd} ≤ 1200 mV), and threshold voltage (250 mV ≤ V_t ≤ 500 mV), which is marked by the shaded region (blue) in Fig. 4. Note that x and y corresponds to, respectively, the supply and threshold voltages. The three vertices of the feasible region are marked by A, B, and C, where the numerical values for A, B, and C describe the reduction in the NPP for a reduction in supply and threshold voltage. The optimal solutions from execution of Algorithm 1 for points A, B, and C are approximately equal to, respectively, 35.4, 46.91, and 44.97, where point A exhibits the minimum reduction in NPP. The optimum supply voltage and threshold voltage at point A is, respectively, 870 mV and 500 mV. Therefore, the optimum solution obtained from the algorithm provides the supply and threshold voltages that correspond to a minimal reduction in the noise performance product.

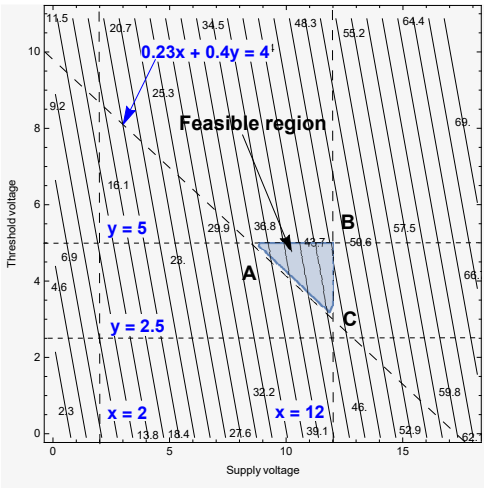

Fig. 4: Feasible region of optimum solution for Test 5. The unit value of x and y correspond to, respectively, 100 mV of supply voltage and 100 mV of threshold voltage.

IV. Conclusions

Noise and performance constrained optimization of the supply voltage is proposed for a given range of threshold voltages, where the variation in noise margins, f_{max}, and threshold voltage are considered. The proposed algorithm is characterized with SPICE simulation for both 130 nm and 45 nm technologies. The algorithm determines the optimum supply and threshold voltages with up to 14% and 8% error in maintaining the constraints for, respectively, NM_{avg} and f_{max}, as determined through SPICE simulation for a 130 nm technology. In addition, the simulation results obtained from a 45 nm technology exhibit variation of up to 0.89× and 8.3× in, respectively, NM_{avg} and f_{max}, as compared to results obtained for a 130 nm inverter.

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