# Robust Near-Threshold Inverter with Improved Performance for Ultra-Low Power Applications

MD Shazzad Hossain and Ioannis Savidis
Department of Electrical and Computer Engineering
Drexel University, Philadelphia, PA 19104
msh89@drexel.edu, isavidis@coe.drexel.edu

***Abstract*—Near-threshold computing (NTC) is a promising technique for low power applications. In this paper, novel circuit techniques for near-threshold computing are developed for improved power, performance, and robustness to noise. Two separate differential signaling based circuits are proposed which outperform CMOS and current-mode logic (CML) operating at near-threshold. The proposed circuits are described as dynamic current-mode logic (DCML) and latched DCML (LDCML). Characterization of the CMOS, CML, and the proposed DCML logic families is performed for area, power, performance and noise immunity at both the nominal and near-threshold operating voltages. At a near-threshold voltage, the DCML logic family reduces the total power by 32% while improving the performance by 82% as compared to CMOS logic. The use of DCML logic also reduces the total power consumption by 92% while improving the performance by 64% as compared to CML logic operating at near-threshold. In addition, the robustness of the proposed logic families to noise is analyzed. At near-threshold voltages, both the noise margins of LDCML is improved by more than 1.4x as compared to CMOS logic.**

## I. Introduction

A promising technique to reduce the power consumption is to scale the supply voltage [1], [2]. Sub-threshold circuits are used for low performance and low-power battery operated portable devices [1]. There are, however, critical limitations with sub-threshold logic, such as severe performance degradation, reduced energy efficiency, susceptibility to variation, increased functional failure, increased vulnerability to noise, and an exponential increase in leakage power as a percentage of the total power [1]–[4].

Near-threshold circuits have gained traction in the research community in the past decade as both the energy efficiency and the performance per watt is improved [5]–[7]. However, most prior work has focused on standard CMOS logic. In addition, the robustness of near-threshold circuits to noise is rarely addressed [8]. Novel robust near-threshold circuits for improved performance and power consumption are therefore proposed for ultra-low power applications.

Prior work has implemented CML for near-threshold computing (NTC), however, the circuits suffer from higher static power consumption and the efficacy is bounded by the operating constraints of the circuits. As an example, CML NTCs are more energy efficient than CMOS only when the operating frequency is higher than 9 GHz [8]. For large circuits, operating close to 9 GHz at a near-threshold supply voltage is not possible with existing technologies. In addition, CMOS based logic suffers from inherent limitations at low supply voltages, which include performance degradation, reduced noise margin, and lower output voltage swing. One potential solution to address the limitations of CMOS and CML is the use of differential DCML based logic circuits at near-threshold voltages. In this paper, two dynamic current-mode logic (DCML) inverters operating at near-threshold are proposed for increased performance, reduced power consumption, and robustness to noise.

The rest of the paper is organized as follows: The proposed DCML logic families are described in Section II. The simulated results are provided in Section III. Concluding remarks are given in Section IV.

## II. Inverter Based on Dynamic current-mode logic (DCML)

The proposed inverters based on dynamic current mode logic (DCML) follow the fundamental principle of both dynamic and current-mode logic circuits [9]. Current-mode logic circuits function with smaller output voltage swing, which is beneficial for low power applications as the delay and switching power are reduced. In addition, the output voltage swing is as equally important as the supply voltage to reduce the dynamic power, as seen from (1). The DCML inverter is shown in Fig. 1. There are two phases of operation: ***1) pre-charge*** and ***2) evaluate***. During the pre-charge phase, both the $Out$ and $\overline{Out}$ nodes are charged to positive $V_{dd}$. During the evaluation phase, depending on the signals on $In$ and $\overline{In}$, $Out$ or $\overline{Out}$ is discharged through, respectively, transistor *N2* or *N1*. In addition, the current ($I_{bias}$) through the gate is regulated by an applied voltage on the tail transistor *N0*, which impacts the input voltage and operating characteristics of the next stage.

The difference in input voltage between $In$ and $\overline{In}$ is considered the ***Input*** ($V_{In}$ - $\overline{V_{In}}$) of the logic gate and the difference between $Out$ and $\overline{Out}$ is considered the ***Output*** ($V_{Out}$ - $\overline{V_{Out}}$) of the gate. However, in order to properly use differential logic, an equal voltage must not be applied to both inputs. For example, if logic low is applied to both $In$ and $\overline{In}$, then both transistors N1 and N2 are turned off and no current flows through the two branches. As a result, an equal voltage appears at both the $Out$ and $\overline{Out}$ nodes. In order to evaluate DCML logic as an inverter at a nominal supply voltage of 1.2 V, logic high is applied to $In$ and logic low to $\overline{In}$. The difference between $In$ and $\overline{In}$ is 1.2 V which is evaluated as logic high. During the evaluation phase, $Out$ discharges through *N2* and the $\overline{Out}$ node remains high. If the output is taken as the difference between $Out$ and $\overline{Out}$,

978-1-4799-5341-7/16/$31.00 ©2016 IEEE

the resulting -1.2 V is evaluated as logic low, and the input signal is inverted. If, however, the output is evaluated as the difference between $\overline{Out}$ and $Out$, the circuit behaves as a buffer. Therefore, explicit inversion is not required for dynamic current-mode logic.

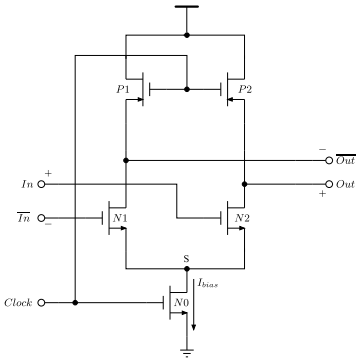



Fig. 1: Implementation of an inverter with dynamic current-mode logic (DCML).

$$P_{switching} = f_{switching} \cdot V_{dd} \cdot V_{switching} \cdot C \quad (1)$$

$$Overdrive\ voltage, (V_{GS} - V_T) = \sqrt{\frac{2I_{bias}}{\mu_n C_{ox} \frac{W}{L}}} \quad (2)$$

The input-output characteristics of the DCML inverter are described by the voltage transfer curve (VTC) shown in Fig. 2. The voltage of the output to the left of *A* represents logic 1 and the voltage of the output to the right of *B* represents logic 0. At the origin, where the ***Input*** is zero (both differential inputs are equal), the same or no current flows through the two branches of the inverter and the voltages at both differential output nodes are equal. The ***Output*** is therefore 0 V and is logically indiscernible (falls halfway between logic 0 and 1). As $In$ is increased with respect to $\overline{In}$, more current flows through branch 2 as compared to branch 1. Similarly, the voltage at $Out$ decreases as charge is grounded, while the voltage at $\overline{Out}$ remains unchanged. As a result, the differential voltage ***Output*** of the logic circuit starts to decrease. The maximum differential value of ***Output*** is achieved when the total charge at one of the output nodes flows through either N1 or N2 (depending on the voltages on $In$ and $\overline{In}$) to ground.

The overdrive voltage given by (2) [10] is an important parameter to regulate the output voltage swing of the chain of inverters. The threshold voltages of both the PMOS and NMOS transistors are, respectively, -0.33 $\pm$ 0.05 V and 0.35 $\pm$ 0.05 V for a 130 nm IBM fabrication process. Depending on the voltages at the terminals and the transistor dimensions, the overdrive voltage varies between 20 to 120 mV and 0 to 100 mV for, respectively, the PMOS and the NMOS devices. For simplicity, the body effect ($V_{SB}$) is assumed to be zero, although it is also possible to control transistor performance through body-biasing at near-threshold voltages [1]. In addition, the channel length modulation $\lambda$ is ignored as the depletion depth surrounding the drain is significantly reduced when the supply voltage is set to 400 mV and the channel length is 130 nm.

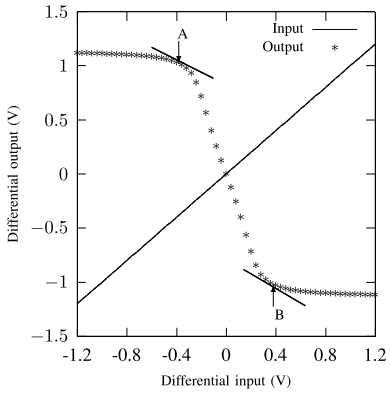



Fig. 2: Voltage transfer curve of a differential inverter.

In order to exploit the robustness of DCML, a family of two logic circuits are proposed for different target applications. The proposed DCML logic families include: 1) standard DCML used for higher performance, and 2) latched DCML (LDCML) used for improved noise immunity. The DCML families differ in the structure of the pull-up network (PMOS devices). However, the operation of both DCML logic circuits is similar.

### A. Latched DCML (LDCML)

The propsoed LDCML inverter is shown in Fig. 3. The inverter includes two minimum sized PMOS transistors (P3 and P4) used to form a latch [11]. The latch preserves the logic level during the evaluation phase if a voltage drop is detected at either of the two output nodes. The area overhead is negligible as minimum sized transistors are used.

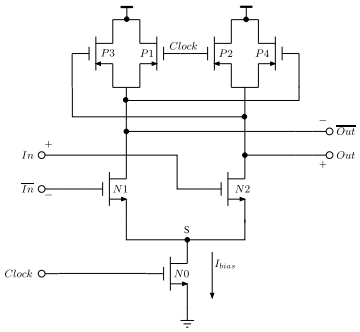



Fig. 3: Latched DCML (LDCML) circuit of an inverter.

## III. Simulated Results

An inverter cell is designed and simulated in each logic family. A four-inverter chain is used to evaluate the total power, area, performance, and noise margins. To our knowledge, no prior work in near-threshold computing has considered the robustness of the circuit to noise. The simulations are performed using an IBM 130 nm technology. The nominal and near-threshold supply voltages are set to, respectively, 1.2 V and 400 mV.

### A. Characterization of power, area, and performance of the logic families

The performance, area, and power consumption of the different logic families are listed in Table 1. From the listed

results, DCML operates at the highest frequency and consumes the least power as compared to all other logic families. Each logic family is designed for minimum area and full swing at the end of the fourth stage at a near-threshold voltage. Among all logic families, DCML is the fastest logic family and CMOS the slowest, where the maximum frequency of operation for the CMOS inverter chain is 63 MHz. Therefore, for a fair comparison, the CMOS and other logic families are analyzed at 60 MHz for area, power, and robustness to noise.

Using a DCML inverter chain at near-threshold reduces the total power consumption by 93% but incurs a 33x penalty in performance as compared to a CMOS inverter chain operating at a nominal supply voltage and with the same area constraint. In addition, at near-threshold, the DCML inverter chain reduces total power consumption by 32% while improving the performance by 82% as compared to a CMOS inverter chain. The total power consumption is reduced by 92% with a 64% improvement in performance when using DCML over CML at a near-threshold supply voltage. In addition, the static power consumption of the DCML logic families is reduced to 0.01% of the total power consumption at a near-threshold voltage when using stacked tail transistors.

TABLE I: Comparison of the performance, area, and power consumption of the four types of inverter chains operating at a 400 mV supply voltage.

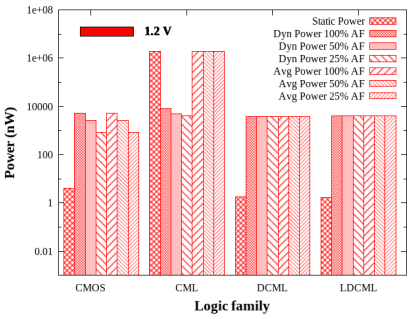
| | CMOS | CML | DCML | LDCML |
|---|---|---|---|---|
| **Max freq. with 4 stages (*MHz*)** | 63 | 70 | 115 | 100 |
| **Area** $(\mu m)^2$ | 2.88 | 10.56 | 4.56 | 4.85 |
| **Static power (*nW*)** | 0.54 | 4550 | 0.2 | 0.19 |
| **Dynamic power (*nW*)** | 544.46 | 300 | 368.8 | 393.81 |
| **Total power (*nW*)** | 545 | 4850 | 369 | 394 |

### *B. Characterization of total power consumption with different activity factors (AF)*

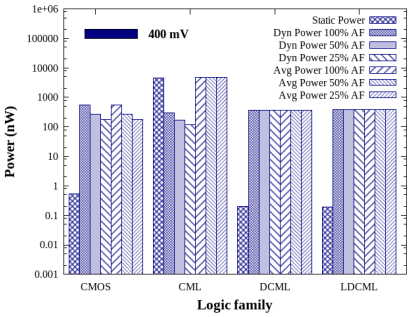
For CMOS logic, dynamic power consumption is reduced with lower activity factor. However, for DCML, the dynamic power does not change with activity factor. CML also shows minor changes in power consumption with a change in activity factor. The power consumption for different activity factors at 1.2 V and 400 mV are shown in, respectively, Figs. 4 (a) and 4 (b). For all logic families and supply voltages, the operating frequency of the inverter chains is set to 60 MHz.

Among all logic families, DCML consumes the minimum static power both at a nominal and near-threshold voltage. At near-threshold, the static power consumption of DCML and LDCML is 0.05% of the total power consumption. The majority of the total power consumed by CML is static for all supply voltages. The majority of the total power consumption in DCML logic families, however, is dynamic. The total power shown in Fig. 4, represents the average power per cycle for different activity factors. The maximum power savings is achieved at higher activity factors.

At near-threshold voltages, an input signal with a period of 16.66 ns is used to produce a 60 MHz operating frequency. The maximum allowed propagation delay is set to 70% of the evaluation phase (85% of the signal period). Including more than four logic stages is difficult when CMOS and CML are used, as the propagation delay exceeds the 70% limit




(a)




(b)

Fig. 4: Power consumption of the logic families for different activity factors when the supply voltage is set to a) 1.2 V, and b) 400 mV.

of the evaluation phase. However, DCML exhibits acceptable propagation delay and output voltage swing with more than four stages, even though there is a 20 to 30 mV reduction in output swing (logical output is still discernible as differential signaling is used). For additional logic stages, the full output voltage swing is achieved with a minor cost in area and power. At near-threshold operating voltages, a larger number of stages is therefore feasible with DCML logic families at a cost of reduced frequency.

### *C. Noise analysis*

The robustness of the logic families to noise is characterized through an analysis of the noise margins at both the nominal and near-threshold supply voltages and with a set frequency of 60 MHz. For the CMOS inverter, a conventional voltage transfer curve (VTC) is used [10]. However, both CML and DCML inverters are evaluated by differential inputs and outputs. The inverter VTC curve therefore represents the difference in the two input and two output signals. The VTCs of the differential logic families are shown in Fig. 5. A comparison of the noise margins for all logic families at both a nominal and near-threshold voltage is shown in Fig. 6. The *NM_H* is always a positive voltage and *NM_L* is always negative for the proposed inverter circuits. However, for ease of comparison and analysis, the absolute value of the *NM_L* is used to calculate the values shown in Fig. 6 for all differential inverters. Both at the nominal and near-threshold voltages the noise margin of the LDCML inverter is better than all other logic families. At near-threshold, the *NM_H* and *NM_L* of a LDCML inverter are, respectively, 228 mV and 564 mV when

an initial differential voltage of 400 mV is applied at the input. In addition, the *NM_H* and *NM_L* of a CMOS inverter are, respectively, 161 mV and 90 mV. Note that for CMOS logic, the *NM_L* is larger than *NM_H* at 1.2 V, but the *NM_H* is larger at 400 mV. The CMOS inverter is therefore the only circuit that exhibits a switch in the relative size of the *NM_L* and *NM_H* when the voltage is reduced from 1.2 V to 400 mV.

For LDCML, the input-output characteristics are sensitive to the polarity and magnitude of initial input voltages (due to the PMOS latch) which results in changes to the noise margins. Inputs with similar voltages maintain a symmetry at the two output nodes unless one of the inputs changes with respect to the other. The VTC with an equal initial differential input voltage is shown in Fig. 5 (LDCML output 1). However, for the analysis of the noise margins, a non-zero initial differential input voltage is chosen, since equal voltages at the inputs results in the logic not functioning as intended. In addition, changing the polarity of the initial differential input to -400 mV changes the *NM_H* and *NM_L* to, respectively, 564 mV and 228 mV (inverted input in Fig. 6). The asymmetric behavior of the noise margins is corrected by increasing the size of the NMOS transistors by 20 fold, resulting in a symmetric output, as shown in Fig. 5 (LDCML output 2). The large NMOS transistors sink current from the output node with a moderate gate voltage, even as the holding PMOS latch is supplying additional charge. As a result, the *NM_L* and *NM_H* are equal regardless of the input polarities. In addition, the asymmetric behavior applies only when the differential input approaches zero, which is not a permitted operating point for the circuit. Therefore, the asymmetric behavior of the noise margins for the LDCML does not effect the circuit operation, while providing additional power savings and speedup as compared to the symmetric implementation. Depending on the applications and specific circuit biasing requirements, the differential inputs are set to either enhance the *NM_L* or *NM_H* of the LDCML inverter.

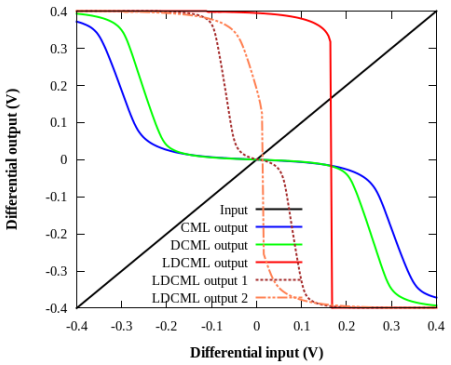



Fig. 5: Simulated VTC of all differential inverters at a 400 mV supply voltage.

## IV. Conclusions

Two DCML logic families are proposed for near-threshold computing and provide improved power, performance, and robustness to noise as compared to CMOS and CML. A DCML inverter operating at a near-threshold voltage reduces the total power consumption by 92% and 32% as compared to, respectively, a CML and a CMOS inverter while also improving the performance. At near-threshold, the maximum operating frequency of the DCML inverter chain is 1.82x times greater as compared to CMOS. In addition, the LDCML inverter provides the best noise margins at a near-threshold voltage among all logic families, producing more than 1.4x the noise margins of a CMOS inverter. The proposed DCML logic families are therefore potential candidates for robust low power circuits. The DCML circuits also permit a larger number of logic stages at near-threshold and provide reduced static power when stacked tail transistors are used.

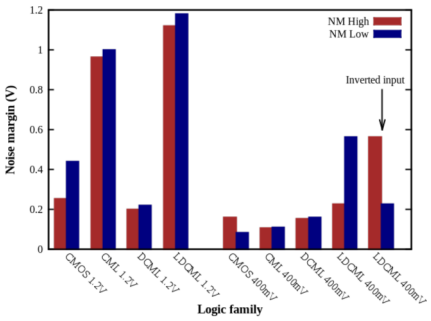



Fig. 6: Comparison of noise margins of logic families at nominal and near-threshold voltages.

## References


[1] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming moore's law through energy efficient integrated circuits," *Proceedings of the IEEE*, Vol. 98, No. 2, pp. 253–266, January 2010.

[2] H. Kaul, M. Anders, S. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar, "Near-threshold voltage (NTV) design: Opportunities and challenges," *Proceedings of the IEEE/ACM Annual Design Automation Conference*, pp. 1153–1158, June 2012.

[3] A. P. Chandrakasan and R. W. Brodersen, "Minimizing power consumption in digital CMOS circuits," *Proceedings of the IEEE*, Vol. 83, No. 4, pp. 498–523, April 1995.

[4] B. H. Calhoun and A. Chandrakasan, "Characterizing and modeling minimum energy operation for subthreshold circuits," *Proceedings of the IEEE International Symposium on Low Power Electronics and Design*, pp. 90–95, August 2004.

[5] D. Marković, C. C. Wang, L. P Alarcon, T. Liu, and J. M. Rabaey, "Ultralow-power design in near-threshold region," *Proceedings of the IEEE*, Vol. 98, No. 2, pp. 237–252, February 2010.

[6] R. G. Dreslinkski, B. Zhai, T. Mudge, D. Blaauw, and D. Sylvester, "An energy efficient parallel architecture using near threshold operation," *Proceedings of the IEEE International Conference on Parallel Architecture and Compilation Techniques*, pp. 175–188, September 2007.

[7] B. Zhai, R. G. Dreslinski, D. Blaauw, T. Mudge, and D. Sylvester, "Energy efficient near-threshold chip multi-processing," *Proceedings of the ACM International Symposium on Low Power Electronics and Design*, pp. 32–37, August 2007.

[8] A. Shapiro and E. G. Friedman, "MOS current mode logic near threshold circuits," *Journal of Low Power Electronics and Applications*, Vol. 4, No. 2, pp. 138–152, June 2014.

[9] M. Yamashina and H. Yamada, "An MOS current mode logic (MCML) circuit for low-power sub-GHz processors," *IEICE Transactions on Electronics*, Vol. 75, No. 10, pp. 1181–1187, October 1992.

[10] E. Salman and E. G. Friedman, *High performance integrated circuit design*, McGraw Hill Professional, 2012.

[11] M. W. Allam and M. Elmasry, "Dynamic current mode logic (DyCML): A new low-power high-performance logic style," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 3, pp. 550–558, October 2001.