Dynamic Current Mode Inverter for Ultra-Low Power Near-Threshold Computing

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***Abstract*—In this paper, novel circuit techniques for near-threshold computing are developed for improved power, performance, and robustness to noise. Three differential signaling based inverters are proposed which outperform CMOS and current-mode logic (CML) operating at near-threshold. The proposed circuits are described as dynamic current-mode logic (DCML), latched DCML (LDCML), and stacked DCML (SDCML). Characterization of the different logic types including CMOS, CML, and the proposed DCML logic families is performed for area, power, performance, and noise margins at both the nominal and near-threshold operating voltages. At near-threshold voltages, the proposed DCML inverter reduces the total power consumption by 32% as compared to a CMOS inverter also operating at near-threshold. The use of a DCML inverter also reduces the total power consumption by 92% as compared to a CML inverter operating at near-threshold. In addition, at near-threshold voltages, both the noise margins of an LDCML inverter are improved by more than 1.4x and the static power consumption of an SDCML inverter is reduced by 88% as compared to a CMOS inverter.**

Keywords: low-power operation; near-threshold circuits; current-mode logic (CML); dynamic current-mode logic (DCML).

I. Introduction

Near-threshold circuits have gained significant traction in the research community in the past decade as the energy efficiency and performance per watt has improved [1]–[3]. Prior research has attempted to exploit sub-threshold logic to significantly reduce the total power consumption. Sub-threshold circuits are used for low performance applications such as wristwatches and hearing aids for increased energy efficiency [3]. There are, however, critical limitations with sub-threshold logic that must be addressed, such as severe performance degradation, susceptibility to variation, increased functional failure, increased vulnerability to noise, and an exponential increase in leakage power as a percentage of the total power [3]–[5]. When the supply voltage is below the threshold voltage (V_{th}), the energy efficiency begins to drop and the performance degrades severely [3]. Operating circuits at slightly above V_{th} is therefore an optimal choice when considering trade-offs between performance, power consumption, and energy efficiency [2], [3]. Most prior work on near-threshold circuits is based on standard CMOS logic. In addition, the reliability and robustness of near-threshold circuits are rarely explored.

CMOS based logic suffers from inherent limitations at low supply voltages, which include performance degradation, reduced noise margin, and lower output voltage swing. One potential solution to mitigate the problems present with CMOS at near-threshold voltages is the use of differential logic circuits [1], [6], [7]. Prior work has proposed differential signaling based current-mode logic (CML) circuits for near-threshold computing (NTC), however, the circuits suffer from higher static power consumption and the efficacy is bounded by the operating constraints of the circuit. As an example, CML NTCs are more energy efficient than CMOS only when the operating frequency is higher than 9 GHz [1]. For large circuits, operating close to 9 GHz at a near-threshold supply voltage is not possible with existing technologies. One potential solution to address the limitations of CMOS and CML is the use of differential DCML based logic circuits at near-threshold voltages.

In this paper, three dynamic current-mode logic (DCML) inverters operating at near-threshold are proposed. The inverter logic circuits are described as dynamic current-mode logic (DCML), latched dynamic current-mode logic (LDCML), and stacked dynamic current-mode logic (SDCML). The area, power consumption, performance, and robustness to noise of the proposed inverters are characterized and compared with current-mode logic and CMOS inverters operating at a near-threshold voltage.

The rest of the paper is organized as follows: The proposed DCML inverters are described in Section II. The simulated results are provided in Section III. Concluding remarks are given in Section IV.

II. Dynamic current-mode logic (DCML) Inverter

The proposed dynamic current mode logic (DCML) inverter is designed based on the fundamental principle of both dynamic and current-mode logic circuits [6]. Current-mode logic circuits function with smaller output voltage swing, which is beneficial for low power applications as the delay and switching power are reduced. In addition, the output voltage swing is as equally important as the supply voltage to reduce the dynamic power, as seen in (1). However, the constant current drawn by the tail transistor of current-mode logic significantly degrades the energy efficiency of the circuit. The concept of dynamic logic is therefore used to reduce the amount of current drawn and more importantly, the large static power consumed by CML.

A DCML inverter is shown in Fig. 1. There are two phases of operation: ***1) pre-charge*** and ***2) evaluation***. During the pre-charge phase, both the Out and $\overline{Out}$ nodes are charged to positive V_{dd}. During the evaluation phase, depending on the signals on In and $\overline{In}$, $\overline{Out}$ or Out is discharged through, respectively, transistor *N1* or *N2*. Explicit inversion is not required in DCML logic. For example, in order to evaluate DCML logic as an inverter, if logic high is applied to In and logic low to $\overline{In}$, the difference between In and $\overline{In}$ is 1.2 V which is evaluated as logic high. During the evaluation phase, Out discharges through *N2* and the $\overline{Out}$ node remains high. If the output is taken as the difference between Out and $\overline{Out}$, the

resulting -1.2 V is evaluated as logic low, and the input signal is inverted. If, however, the output is evaluated as the difference between $\overline{Out}$ and Out, the circuit behaves as a buffer.

$$P_{switching} = f_{switching} \cdot V_{dd} \cdot V_{switching} \cdot C \quad (1)$$

$$Overdrive\ voltage, (V_{GS} - V_T) = \sqrt{\frac{2I_{bias}}{\mu_n C_{ox} \frac{W}{L}}} \quad (2)$$

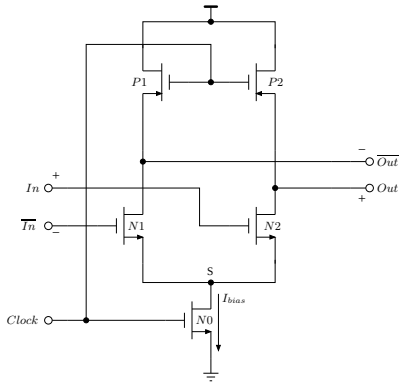


Fig. 1: An inverter circuit implemented with dynamic current-mode logic.

The input-output characteristics of the DCML inverter are described by the voltage transfer curve (VTC) shown in Fig. 2. The ***Input*** and ***Output*** of the inverter is considered as the difference between, respectively, In and $\overline{In}$ and Out and $\overline{Out}$.

The output voltage values above point A represent logic 1 and the output voltage values below point B represent 0. When both differential inputs are equal (at the origin of the VTC), the same or no current flows through the two branches of the inverter and the voltages at both differential output nodes are equal. The ***Output*** is therefore 0 V and is logically indiscernible (falls halfway between logic 0 and 1). The maximum differential value of ***Output*** is achieved when the total charge at one of the output nodes flows through either N1 or N2 (depending on the voltages on In and $\overline{In}$) to ground.

The overdrive voltage given by (2) [8] is an important parameter to regulate the output voltage swing of the chain of inverters. The threshold voltages of both the PMOS and NMOS transistors are, respectively, -0.33 ± 0.05 V and 0.35 ± 0.05 V for a 130 nm IBM CMOS technology. Depending on the voltages at the terminals and the transistor dimensions, the overdrive voltage varies between 20 to 120 mV and 0 to 100 mV for, respectively, the PMOS and NMOS devices. For simplicity, the body effect (V_{SB}) is assumed to be zero, although it is also possible to control transistor performance through body-biasing at near-threshold voltages [3]. In addition, the channel length modulation λ is ignored as the depletion depth surrounding the drain is reduced when the supply voltage is set to 400 mV.

In order to exploit the robustness of dynamic current-mode logic, three versions of DCML are proposed to address different target applications. The proposed DCML logic families include: 1) standard dynamic current-mode logic (DCML) used for high performance, 2) latched dynamic current-mode logic (LDCML) used for improved noise immunity, and 3) stacked dynamic current-mode logic (SDCML) used to reduce leakage. The

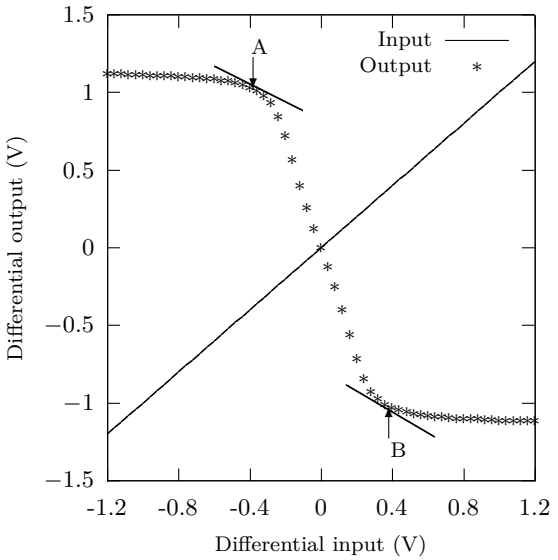


Fig. 2: Voltage transfer curve of a differential inverter.

DCML families differ in the structure of the tail and holding transistors. However, the operation of all DCML inverters are similar. The three DCML logic families are compared with CMOS and CML for performance, area, power consumption, and robustness to noise. The circuit operation and description of LDCML and SDCML inverters are provided in the next two subsections.

A. Latched dynamic current-mode logic (LDCML)

The proposed LDCML inverter is shown in Fig. 3, which includes two minimum sized PMOS transistors (P3 and P4) used to form a latch [7] in parallel with the two PMOS load transistors found in DCML. The latch is used to preserve the voltage on the output during the evaluation phase. The area and power overhead of the additional PMOS transistors are negligible since minimum sized transistors are used.

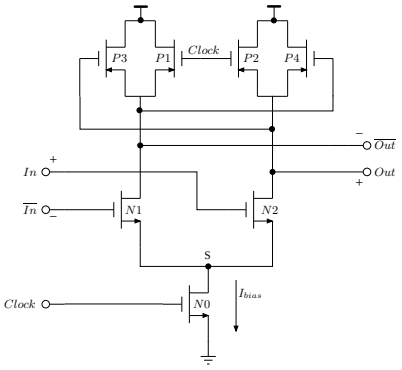


Fig. 3: Latched DCML (LDCML) circuit of an inverter.

B. Stacked dynamic current-mode logic (SDCML)

The SDCML logic is similar to DCML except that two series connected tail transistors are used instead of a single tail transistor. The stacked tail transistors reduce the leakage current in the circuit [9]. For SDCML, two equal sized transistors *N01* and *N02* replace *N0* in Fig. 1. The supply voltage *Vdd* is applied to

the gate of both bias transistors. The applied voltage to the bias transistors can be modified to modulate the circuit behavior.

III. Simulated Results

An inverter cell is designed and simulated in each logic family. A four-inverter chain is used to evaluate the total power, area, performance, and noise margins. Prior work on near-threshold computing has not considered the robustness of the circuit to noise. The nominal supply voltage is set to 1.2 V for all logic families. The supply voltage is set to 400 mV when operating at near-threshold.

A. Characterization of power, area, and performance among different logic families

The performance in terms of maximum operating frequency, area, and power consumption of the different logic families are listed in Table I, where DCML outperforms all other logic families. From the listed results, DCML operates at the highest frequency and consumes the least power from all logic families. Each logic family is designed for minimum area and full swing at the end of the fourth stage when operating at a near-threshold voltage. Among all logic families, DCML is the fastest and CMOS the slowest. The maximum operating frequency of the CMOS inverter chain is 63 MHz. Therefore, to fairly compare the logic families, the operating frequency is set to 60 MHz and the area, power, and robustness to noise is analyzed. At a 60 MHz operating frequency and 400 mV supply voltage, the DCML inverter chain consumes 32% less power than the CMOS inverter chain. Using a DCML inverter chain at a near-threshold voltage reduces the total power consumption by 93% but incurs a 33x penalty in performance as compared to a CMOS inverter chain operating at a nominal supply voltage of 1.2 V and with the same area constraint. In addition, the total power consumption is reduced by 92% with a 64% improvement in performance when using DCML over CML at a near-threshold supply voltage.

For applications with strict static power requirements, SDCML provides the best solution. At near-threshold voltages, the CMOS inverter consumes 9.64x times the static power as compared to an SDCML inverter. In contrast, the "always on" tail transistor of the CML inverters increases the overall static power consumption. Therefore, at near-threshold voltages, the CML inverters consume 81250x (4550 nW) times the static power as compared to SDCML inverters, as listed in Table I. In addition, the static power consumption of the SDCML inverter is reduced to 0.01% of the total power consumption at a near-threshold voltage.

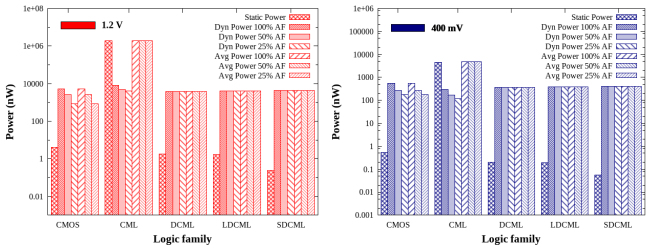
TABLE I: Performance, area, and power comparison at a 400 mV supply voltage.

	CMOS	CML	DCML	LDCML	SDCML
Max freq. with 4 stages (*MHz*)	63	70	115	100	90
Area (μm^2)	2.88	10.56	4.56	4.85	5.9
Static power (*nW*)	0.54	4550	0.2	0.19	0.056
Dynamic power (*nW*)	544.46	300	368.8	393.81	409.94
Total power (*nW*)	545	4850	369	394	410

B. Characterization of total power consumption for different activity factors (AF)

Dynamic power consumption is reduced with lower activity factor for CMOS logic. However, for DCML, the dynamic power does not change with activity factor. DCML circuits are therefore beneficial to reduce noise on the power delivery network. CML also exhibits minor changes in power consumption with a change in activity factor. The power consumption for different activity factors is shown in Fig. 4. The nominal 1.2 V and near-threshold 400 mV supply voltages are shown in Fig. 4(a) and 4(b), respectively. For all logic families and supply voltages, the operating frequency of the inverter chain is set to 60 MHz.

Among all logic families, SDCML consumes the least static power both at a nominal and near-threshold voltage. The majority of the total power consumed by CML is static for all supply voltages. The majority of the total power consumption of DCML logic families, however, is dynamic. The average power shown in Fig. 4, represents the total power consumed per cycle for different activity factors. The maximum power savings is achieved at higher activity factors. An input signal with a period of 8.33 ns is used to produce a 60 MHz operating frequency at near-threshold voltages. The maximum allowed propagation delay is set to 5.831 ns (70% of the signal period) for the DCML logic families.



(a) (b)

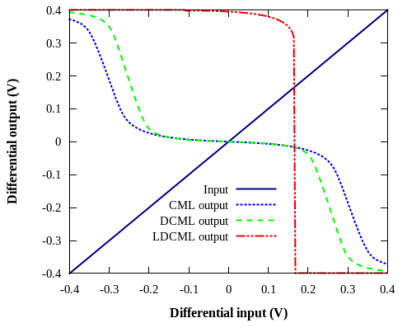
Fig. 4: Power consumption of the logic families for different activity factors when the supply voltage is set to a) 1.2 V, and b) 400 mV.

C. Noise analysis

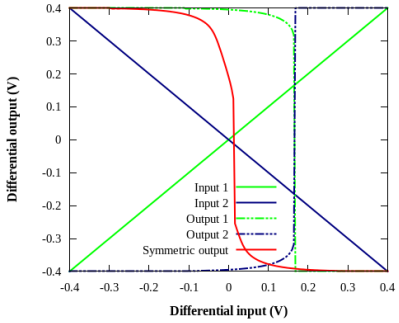
An analysis of the noise margins is done at both the nominal and near-threshold supply voltages at a set frequency of 60 MHz to characterize the robustness of the logic families. A conventional voltage transfer curve (VTC) is used to determine the noise margin of the CMOS inverter [8]. However, CML and DCML inverters are evaluated by differential inputs. As the inverter ***Input*** and ***Output*** are both differential signals, the VTC curve represents the difference in the two input and two output signals, as shown in Fig. 5 (a).

A comparison of the noise margins for all logic families at both a nominal and near-threshold voltage is shown in Fig. 6. The noise margin high (NM_H) is always a positive voltage, and the noise margin low (NM_L) is always negative for the proposed inverter circuits. However, to simplify the comparison and analysis of the logic families, the absolute value of the NM_L is used to calculate the values shown in Fig. 6 for all DCML inverters. Both at a nominal and near-threshold voltage, the noise margin of the LDCML inverter is greater than all other logic families. At near-threshold, the NM_H and NM_L of an LDCML inverter are, respectively, 228 mV and 564 mV for a differential input starting at 400 mV and finishing at -400 mV. In comparison, the NM_H and NM_L of a CMOS inverter are, respectively, 161 mV and 90 mV.

For LDCML, one of the differential input paths dominates the other based on the initial input voltages on the inverter (due to the PMOS latches). Therefore, the initial zero voltage on the N1 transistor results in a differential NM_L of 564 mV, which is higher than the voltage applied to any single input. An analysis of differential inputs starting with the opposite



(a)



(b)

Fig. 5: Simulated VTC of a) all differential inverters at a 400 mV supply voltage, and b) an LDCML inverter at a 400 mV supply voltage for the two directional input polarity sweeps and two NMOS transistor sizes.

polarity (differential input of -400 mV) result in a NM_H of 564 mV and NM_L of 228 mV. The voltage transfer curve (VTC) of an LDCML inverter with opposite input polarities is shown in Fig. 5 (b) and the corresponding noise margins are shown in Fig. 6 (marked as inverted input). In Fig. 5 (b), Input 1 represents the differential input with values for In and $\overline{In}$ initially set to, respectively, 400 mV and 0 V. Input 2 represents the opposite differential input condition where the values of In and $\overline{In}$ are initially set to, respectively, 0 V and 400 mV. The asymmetric behavior of the VTC is corrected by increasing the size of the NMOS transistors by 20 fold, resulting in a symmetric output, as shown in Fig. 5 (b). The large NMOS transistors sink current from the output node with a moderate gate voltage, even as the holding PMOS latch is supplying additional charge. As a result, the NM_L and NM_H are equal regardless of the input polarities. In addition, the asymmetric behavior applies only when the differential input approaches zero, which is not a permitted operating point for the circuit. Therefore, the asymmetric behavior of the noise margins for the LDCML does not effect the circuit operation, while providing additional power savings and speedup as compared to the symmetric implementation. Depending on the applications and specific circuit biasing requirements, the differential inputs are set to either enhance the NM_L or NM_H of the LDCML inverter.

IV. Conclusions

Three DCML inverters are proposed for near-threshold computing that provide improved power, performance, and robustness to noise as compared to CMOS and CML inverters. The proposed DCML inverter operating at a near-threshold voltage

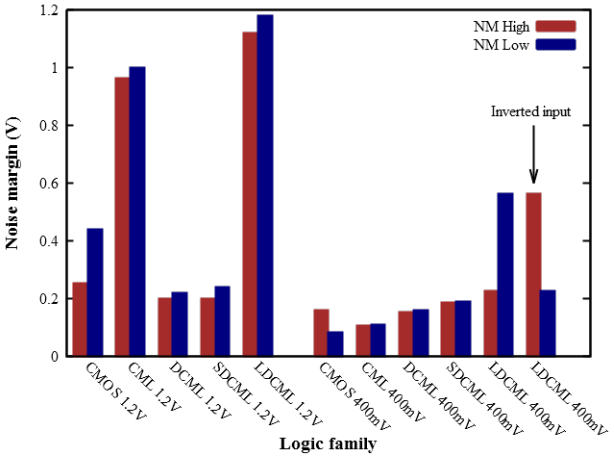


Fig. 6: Comparison of the noise margins of the logic families.

reduces the total power consumption by 92% as compared to a CML inverter while also improving performance by 64%. In addition, the total power consumption of the DCML inverter chain is reduced by 32% as compared to a CMOS inverter chain at near-threshold. At near-threshold, the maximum operating frequency of the DCML inverter chain is 1.83x times greater than CMOS. The LDCML inverter provides the largest noise margins at near-threshold operation among all logic families, with a 1.4x larger high (or low) and 6.7x larger low (or high) noise margin as compared to a CMOS inverter. The SDCML reduces static power by 88% as compared to a CMOS inverter operating at near-threshold.

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