Implementation of Analog Systems on a Reconfigurable Array

Ziyi Chen
Department of Electrical and Computer Engineering
Drexel University
Philadelphia, PA
Email: ziyi.chen@drexel.edu

Ioannis Savidis
Department of Electrical and Computer Engineering
Drexel University
Philadelphia, PA
Email: isavidis@coe.drexel.edu

***Abstract*—Reconfigurable analog circuits are an emerging research topic of interest. In this paper, a noval field-programmable analog array (FPAA) architecture is proposed that provides flexibility in prototyping various analog circuits. Two configurable analog block (CAB) topologies are developed that implement, respectively, single-ended mode and differential mode analog circuits. A global feedback network is implemented to support closed loop systems. A synthesis flow is proposed to map targeted analog circuits onto the FPAA fabric. The FPAA core contains 498 routing switches and 14 fixed global interconnects while occupying an area of 0.1 mm^2 in a 65 nm CMOS process. Circuits implemented on the FPAA include a two-stage operational amplifier (op amp), a lossy integrator, a bandpass filter, a ring oscillator, and a frequency divider. The power consumption of the FPAA is approximately 24.6 mW when operating at a supply voltage of 1.2 V.**

I. Introduction

Due to the high cost of designing and fabricating an analog integrated circuit (IC) in advanced technology nodes, prototyping a targeted design on a programmable IC has gained research interest in both industry and academia. While the development of the field-programmable gate array (FPGA) has allowed for reconfiguration of different digital circuits, programming an analog IC is far from mature. Unlike FPGAs that include logic gates, flip-flops, and look-up tables (LUTs) to implement digital circuits of any Boolean function, analog ICs include large variations in topology as well as in target specifications and applications, which are, therefore, hard to generalize into a single architecture.

The field-programmable analog array (FPAA) is the analog counterpart to the FPGA, and provides reconfigurability into different analog circuits through programmable routing switches. Prior work on the development of the FPAA includes transistor-level topologies [1], floating-gate based topologies [2], and a transconductance cell based topology [3], all of which target a specific application and circuit scale.

The configurable analog block (CAB) is the primary sub-block of the FPAA fabric. The CAB contains transistors, coarse grained analog modules including amplifiers, passive devices (resistors and capacitors), and routing switches that provide the ability of the fabric to reconfigure into small scale analog circuits. The global routing switches and interconnects are used to form the connection between multiple CABs, which permits the implementation of larger scale analog circuits. Although transistor level reconfiguration [4] provides the greatest flexibility, the circuit scale and bandwidth are limited due to the extensive use of routing switches. However, coarse grained analog blocks allow for large scale application at the cost of less flexibility within individual CABs.

There are two types of interconnect methodologies between CABs, switch-based and switch-less. Although routing switches provide programming flexibility [2], the reduction in bandwidth due to the switches limits the maximum operating frequency of the FPAA. Implementing a switch-less routing network [3] increases the bandwidth at the cost of less reconfigurability.

In this paper, a novel FPAA architecture is proposed. The routing switches are implemented within the CAB to enhance the routing flexibility, where the functionality of the CAB is unspecified prior to programming. The switch-less routing strategy is applied between the CABs to limit the impact on the bandwidth due to the global routing network. The analog circuits implemented on the FPAA include a two-stage op amp, a lossy integrator, a bandpass filter, a ring oscillator, and a frequency divider. The architecture of the FPAA is described in Section II. The characterization of the bandwidth of the FPAA is provided in Section III. A synthesis flow to rapidly implement targeted designs on the FPAA fabric is presented in Section IV. The implementations of analog circuits that utilize multiple CABs are described in Section V. A comparison with prior FPAA fabrics is provided in Section VI. Some concluding remarks are provided in Section VII.

II. Architecture of FPAA

The architecture of the proposed FPAA is shown in Fig. 1, where 36 CABs are placed into a 6x6 matrix. For each column, two I/O ports are utilized to provide direct access to the input and output of the CABs. In addition, two types of CABs are included to support both differential mode and single-ended mode analog circuits. A global feedback network is added to facilitate reconfiguration of closed loop systems with positive or negative feedback.

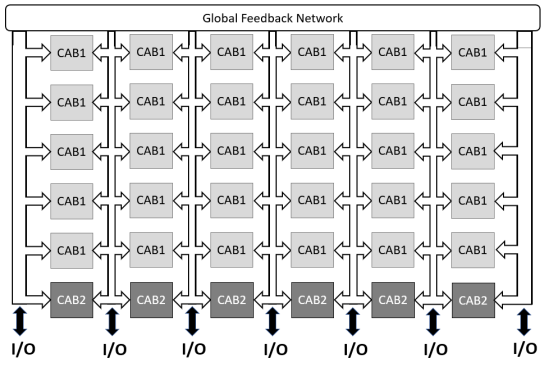
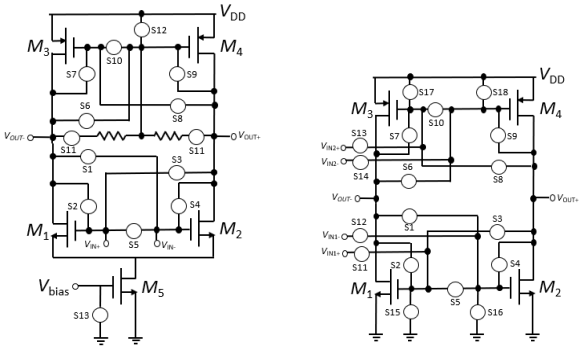


Fig. 1. The FPAA core is organized into a 6x6 CAB matrix. There are two types of CABs, one to support differential mode operation and the other to support single-ended mode operation.

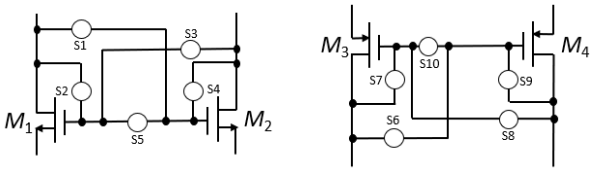
A. Differential Mode CAB

The schematic of the differential mode CAB is shown in Fig. 2a, which consists of one NMOS transistor pair, one PMOS transistor pair, one NMOS current source, and 13 routing switches. The schematic of a generic NMOS transistor pair is shown in Fig. 3a, where switches S1 to S5 are implemented to program transistors M1 and M2 into four different configurations as shown in Fig. 4. The same general topology is provided for PMOS transistor pairs. Switch S11 in Fig. 2a is utilized to provided common-mode feedback (CMFB), while S12 and S13 are added to turn off the CAB completely by pulling the gate voltage of the NMOS transistor to ground and the gate voltage of the PMOS transistor to V_{DD}.



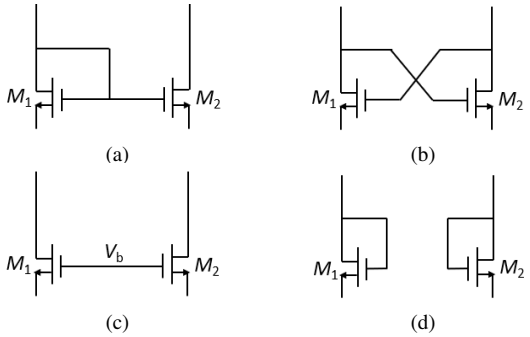
(a) (b)

Fig. 2. Schematic of a (a) differential mode CAB (CAB1), and (b) single-ended mode CAB (CAB2). CAB1 includes 13 routing switches, in addition to four possible configurations of the transistor pair. S11 is added to provide common-mode feedback, while S12 and S13 completely turn off CAB1. CAB2 includes 18 routing switches. S11 to S14 isolate the global switch-less interconnects and the gates of transistors M_1 to M_4. S15 to S18 turn off the CAB.



(a) (b)

Fig. 3. Schematic of the (a) reconfigurable NMOS pair and (b) reconfigurable PMOS pair. Each pair utilizes five reconfigurable routing switches.



(a) (b)

(c) (d)

Fig. 4. Topologies implemented with a single NMOS transistor pair include a (a) current mirror, (b) regeneration loop, (c) current source pair, and (d) diode-connected pair. The same topologies are implemented with the PMOS transistor pair.

B. Single-ended Mode CAB

The schematic of a single-ended mode CAB (CAB2) is shown in Fig. 2b, which includes one NMOS transistor pair, one PMOS transistor pair, and 18 routing switches. Switches S1 to S5 and transistors M1 and M2 form the reconfigurable NMOS pair, while switches S6 to S10 and transistors M3 and M4 form the reconfigurable PMOS pair. Switches S15 to S18 are utilized to turn off the CAB, while switches S11 to S14 are added to isolate the gates of transistors M1 to M4 and the global switch-less interconnects. The single-ended mode operation is implemented by utilizing only half of the transistors and switches. For example, when transistors M1 and M2 are utilized as a common-source amplifier, S5 and S10 are turned off to isolate the applied voltage to the gate of the two NMOS transistors and the two PMOS transistors, respectively. Switches S16 and S18 are then turned on, which permits use of only the transistors on the left half of the CAB. Note that each CAB2 allows for at most two single-ended mode circuits by utilizing transistors from both the left half and right half of the CAB topology, with switches S5 and S10 isolating the gate voltages of each half of the CAB.

C. Global Feedback Network

In order to implement closed loop systems that require positive or negative feedback, a global feedback network is developed as shown in Fig. 5. The input and output ports of the CABs from the same column are connected to the feedback network using 8 routing switches. Two parallel paths are included within the feedback network to facilitate differential mode operation. Positive feedback is provided by connecting two switch-less interconnects with the same polarity, while negative feedback is provided by connecting two switch-less interconnects with opposing polarity. Since the global feedback network connects to all the CABs within the CAB matrix, the implementation of feedback networks between any two columns of CABs is realizable.

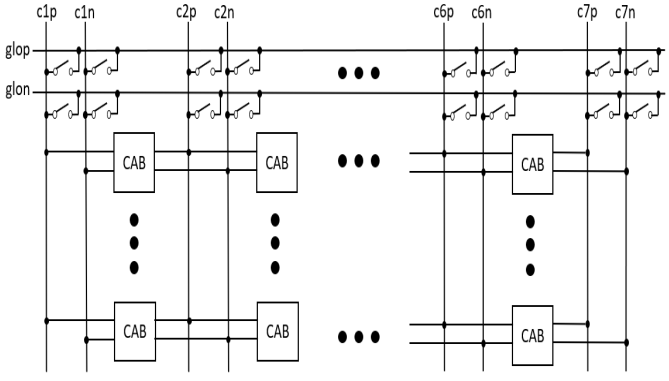


Fig. 5. Schematic of global feedback network. The feedback network consists of 2x28 switches that support multi-CAB level feedback throughout all six columns of the CAB matrix.

III. Bandwidth of the FPAA

In this section, the bandwidth of circuits implemented on the FPAA is analyzed. Although routing switches provide flexibility and programmability to the FPAA fabric, the on resistance and parasitic capacitance of the switches limits the bandwidth of the implemented analog circuits. The resistance and capacitance of the routing switches is first characterized in

Section III-A, followed by a comparison of the achieved bandwidth between a fully custom analog circuit and a functionally equivalent reconfigured implementation in Section III-B.

A. Parasitic Resistance and Capacitance of Switches

The routing switches contribute parasitic resistance and capacitance to the internal nodes of the CABs. The four models of the parasitic impedances of a reconfigurable NMOS transistor pair shown in Fig. 6 represent four different configurations of the routing switches. For each parasitic model, the capacitors C_1 and C_2 represent the parasitic capacitance from switches S1, S2 and S3, S4 respectively, with the topology of the switches as shown in Fig. 3a. Capacitors C3 and C4 represent the parasitic capacitance from switches S2, S3, S5 and S1, S4, S5, respectively. Each resistor represents the on resistance of the routing switch, which is 150 Ω for a *W/L* ratio of 10 µm over 130 nm. The extracted parasitic capacitance from the layout was 38 fF for C_1 and C_2 and 41 fF for C_3 and C_4.

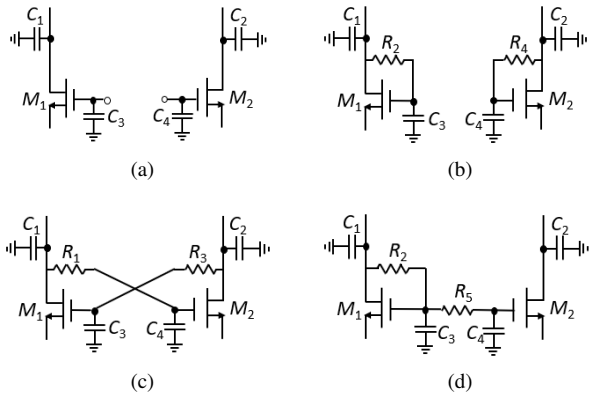


Fig. 6. Parasitic model of four configurations of a NMOS transistor pair that include (a) differential input pair, (b) diode-connected pair, (c) regeneration loop pair, and (d) current mirror pair.

B. Bandwidth Comparison between Fully Custom and Reconfigured Circuit

The bandwidth is characterized by reconfiguring the FPAA fabric into different circuit topologies and comparing the characterized bandwidth with the corresponding bandwidth of a fully custom implementation. The differential mode CAB is programmed to implement an op amp with a current mirror load, an op amp with a current source load, and an op amp with common-mode feedback. The comparison of the 3-dB bandwidth is provided through the results listed in Table I, with a minimum and maximum drop in bandwidth of approximately 2.3 GHz and 3.84 GHz, respectively. The 3-dB bandwidth for all configurations is greater than 800 MHz despite the significant drop in the bandwidth due to the parasitic impedance of the routing switches.

Similarly, the single-ended mode CAB is reconfigured into a common source amplifier to characterize the performance. The AC analysis of the amplifier implemented on the reconfigurable FPAA fabric indicates a 3-dB bandwidth of 3.17 GHz, while the fully custom amplifier provides a 3-dB bandwidth of 27.5 GHz. The significant drop in bandwidth is due to the parasitic impedance of the additional routing switches that isolate the transistor gates and the global switch-less interconnect.

TABLE I
3-DB BANDWIDTH COMPARISON OF BASELINE AND RECONFIGURABLE AMPLIFIERS

Implementation		3-dB Bandwidth of	
		Reconfigured	Baseline
Op-Amp	Current Mirror Load	887 MHz	3.2 GHz
	Current Source Load	958 MHz	4.8 GHz
	Current Source Load CMFB	1.39 GHz	4.7 GHz

IV. SYNTHESIS METHODOLOGY

Although algorithms and methodologies for the mapping of digital circuits onto the FPGA are mature and well developed, there are no general principles for mapping analog circuits onto the FPAA due to the distinct topologies and architectures of the various analog circuits. In this section, a CAB-oriented flow is presented to facilitate rapid implementation of target analog circuit designs on the FPAA.

A. Placement

Mapping a targeted design on the FPAA fabric first requires the placement of the sub-blocks of a circuit on different CABs. For example, a three-stage ring-oscillator requires three CABs connected in series. Since each column of the CAB matrix contains six CABs, the unneeded CABs are turned off by removing the current source. Note that selecting more than one CAB from the same column is supported, which is useful in designing a G*m*-C based analog circuit [5]. For a 6x6 CAB matrix, the FPAA supports a target circuit with at most six sub-blocks, where each block is distibuted across at most six CABs connected in parallel.

B. Routing

In order to rapidly implement and reconfigure individual CABs, a library containing various possible configurations of a single CAB is developed. For each selected CAB, the user determines the desired configuration from the library. A list of corresponding active switches for the given configuration is selected for SPICE simulation as indicated by Algorithm 1. All the CABs within the CAB matrix are labeled with row-major order and programmed sequentially. The complete synthesis flow is shown in Fig. 7. After setting the routing switches within the CABs, the CAB biases and the global feedback network are programmed accordingly, which is followed by SPICE simulation utilizing an ocean script.

V. UTILIZATION OF THE MULTI-CAB ARRAY

In this section, reconfigured circuits utilizing multiple CABs are analyzed. Implemented circuits include a two-stage op amp, a lossy integrator, a biquad bandpass filter, a ring oscillator, and a frequency divider

A. Two-stage Op Amp

The operational amplifier is the fundamental building block of many analog systems including phase-locked loops (PLLs), analog to digital converters (ADCs), and radio frequency (RF) transceivers. The FPAA supports different topologies of op amps by programming the routing switches within the differential mode CABs. While an individual CAB is reconfigured into a single-stage op amp, implementing a multi-stage op amp requires multiple CABs. A two-stage op amp, as shown in Fig. 8, is reconfigured by utilizing one differential mode CAB (CAB1) and one single-ended mode CAB (CAB2). A CAB1 from the CAB matrix is first selected and configured

Algorithm 1: Synthesis algorithm for FPAA

Input: queue Q containing all sub-blocks (C_1, C_2,.. C_N)
Output: switch list S
Function `Placement()`:
    get the length of Q
    select equal number of CABs
Function `Routing()`:
    initialize empty switch list S
    for *each CAB in array* **do**
        if *CABi is selected* **then**
            CabMode = pop(Q)
            S.pushBack(getKeys(CabMode))
        else
            CabMode = OFF
            S.pushBack(getKeys(CabMode))
return S

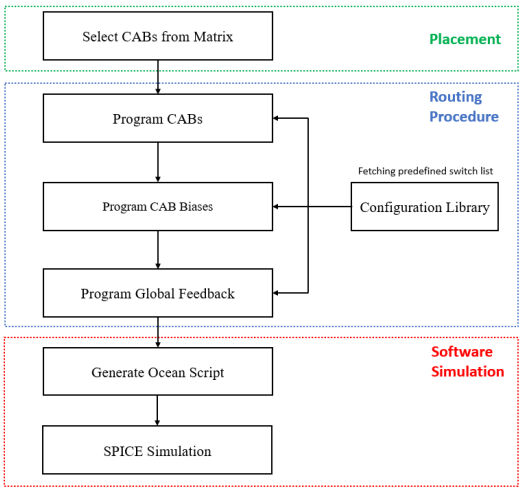


Fig. 7. Design flow of implementing analog circuits on the FPAA. After determining the configuration of the CABs, the CAB biases, and the global feedback network, a list containing all the configuration data is generated. The configuration list is then compiled into an ocean script for simulation.

to implement a single-stage op amp acting as a high gain stage. The high-swing second stage is implemented in a CAB2 located in the second column of the CAB matrix. The characterized gain of the configured two-stage op amp is shown in Fig. 9. A total DC gain of 37.8 dB is provided, with the first stage generating a DC gain of 20 dB. The 3-dB bandwidth of the two-stage op amp is approximately 60 MHz.

B. Lossy Integrator

A lossy integrator is a programmable low pass filter utilizing two transconductance cells as shown in Fig 10. The FPAA is reconfigured into a lossy integrator by selecting CAB1s from two adjacent columns of the CAB matrix. The selected CAB1s are configured into a single stage op amp with common-mode feedback (CMFB). Since the activated CABs from the same column are connected in parallel, the transconductance of the G_{m} cell depends on the number of utilized CABs. The transfer function of the lossy integrator is given by

$$T(s) = \frac{\frac{G_{m1}}{G_{m2}}}{\frac{sC_p}{G_{m2}} + 1}, \tag{1}$$

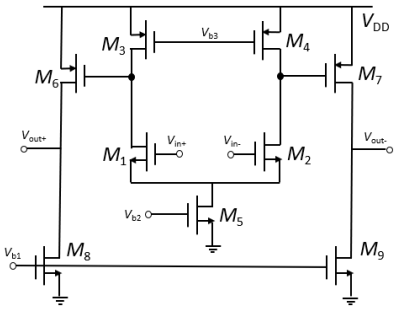


Fig. 8. Schematic of a two-stage op amp. The first stage, a single stage op amp, provides a high gain. The second stage is implemented as a common source amplifier that provides high swing.

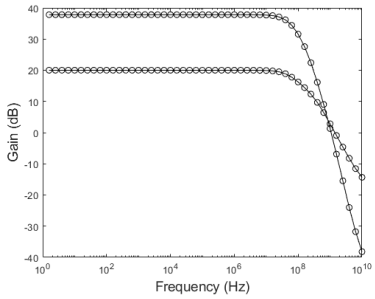


Fig. 9. Transient simulation of a two-stage op amp. The first stage provides a DC gain of 20 dB. The total DC gain of the reconfigured two-stage op amp is 37.8 dB.

where capacitance C_p depends on the output capacitance of the CABs from the first selected column, the input capacitance of the second selected column, and the parasitic capacitance from the switch-less interconnect. The characterized AC response of the lossy integrator is shown in Fig. 11. The minimum gain is provided when both G_{m1} and G_{m2} include one activated CAB. The maximum gain is achieved by utilizing four CABs in parallel to implement G_{m1} while G_{m2} is implemented utilizing only one CAB.

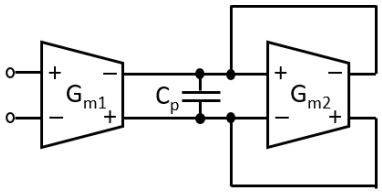


Fig. 10. Schematic of a lossy integrator. Two G_{m} cells are implemented on two separate CAB1s.

C. Ring Oscillator

A ring oscillator is a critical component of a clock generator circuit, phase-locked loop, and data recovery circuit. The FPAA utilizes multiple CAB1s configured to implement a differential mode ring-oscillator. Different from the inverter-based ring oscillator, which utilizes a single-ended signal, a differential mode ring oscillator includes multiple stages of single-stage op amps with diode connected loads. Utilizing a differential signal also allows for an even number of stages, which provides extra flexibility in tuning the oscillating frequency. The schematic of a four stage ring-oscillator is

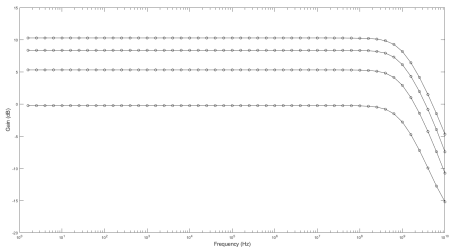


Fig. 11. AC characterization of a lossy integrator. The range of tunable gains is from 0 dB to 10 dB.

shown in Fig. 12, where each stage is configured in a CAB1 selected from individual columns of the CAB matrix. The forward connections between the stages is achieved through the switch-less interconnect, while the feedback between the output of the last stage and the input of the first stage utilizes the global feedback network. The transient simulation of a configured six-stage ring oscillator is presented in Fig. 13a, which indicates a peak-to-peak voltage swing of 0.45 V. The oscillating frequency as a function of the number of stages is shown in Fig. 13b, where a maximum frequency of 478 MHz and a minimum frequency of 207 MHz is provided when the ring oscillator is programmed as three stages and six stages, respectively.

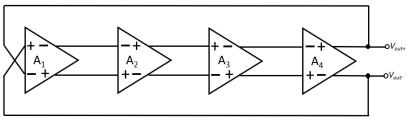
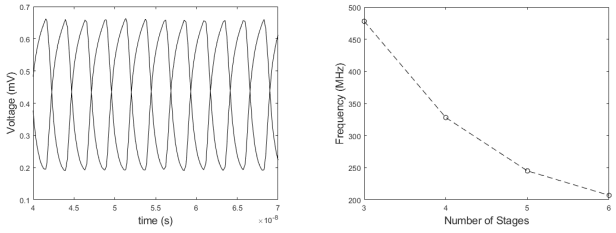


Fig. 12. Schematic of a four-stage ring oscillator. An even number of stages is possible due to the utilization of differential mode signals.



(a) (b)

Fig. 13. Simulation of a differential ring oscillator to characterize (a) the transient response of six-stages, which oscillates at a frequency of 207 MHz, and (b) the oscillating frequency as a function of the number of stages, with three to six stages analyzed.

D. Second Order Biquad Filter

The biquad filter is a G_m-C bandpass filter with tunable peak gain and center frequency. The schematic of a second order biquad filter is shown in Fig. 14, which includes four G_m cells. The FPAA is configured into a biquad filter by selecting four consecutive columns of the CAB matrix, where the CAB1s from each column are utilized and configured into a single-stage op amp with CMFB. The transconductance is tuned by turning on a variable number of CAB1s in a given column, with the tuning range set by activating a single CAB1 or multiple CAB1s connected in parallel. While the negative feedback for G_{m2} is applied through the routing switches (S_2 and S_4 in Fig. 2a) within the CAB, the positive feedback between the output ports of G_{m4} and the input ports of G_{m2} is applied through the reconfiguration of the global feedback network. The transfer function of a second-order biquad filter is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}\frac{C_2}{C_1}S}{S^2 + \frac{g_{m2}}{C_1}S + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{2}$$

$$= K\frac{\frac{\omega_0}{Q}S}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \text{ for} \tag{3}$$

$$K = \frac{g_{m1}}{g_{m2}},\ \frac{\omega_0}{Q} = \frac{g_{m2}}{C_1} \text{ and } \omega_0^2 = \frac{g_{m3}g_{m4}}{C_1C_2}, \tag{4}$$

where K represents the peak gain, ω_0/Q the bandwidth, Q the quality factor, and ω_0 the center frequency. The analysis of a configured biquad filter indicates a tunable peak gain that ranges from -9 dB to 8 dB with a center frequency of approximately 1.5 GHz as shown in Fig. 15.

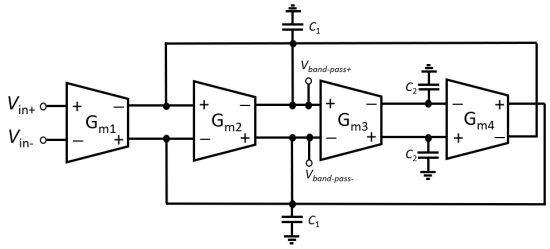


Fig. 14. Schematic of a second-order biquad filter. Each G_m cell consists of one or multiple CABs from a single column of the CAB matrix. The negative feedback for G_{m2} is set through the feedback switches within the CAB. The positive feedback between G_{m4} and G_{m2} is achieved through the global feedback network.

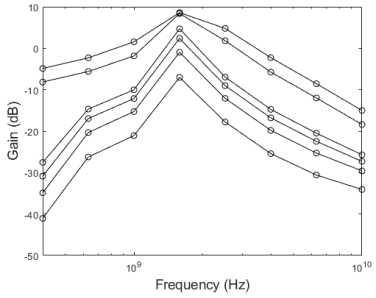


Fig. 15. Simulation of the second-order biquad filter, where the bandwidth and peak gain are tuned by adjusting G_{m1} and G_{m2}.

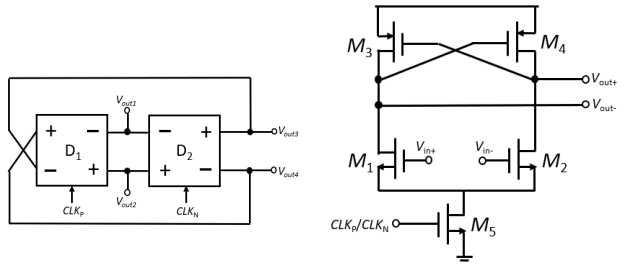
E. Frequency Divider

A frequency divider is a continuous-time analog circuit that generates output signals with half of the input frequency. A differential mode frequency divider is useful in generating quadrature output signals that are 90 degree phase shifted. The frequency divider is used across multiple applications including clock generation and quadrature phase shift keying (QPSK) modulation. The schematic of a differential mode frequency divider is shown in Fig. 16a, which consists of two differential dynamic latches. Two CAB1s are utilized to implement a frequency divider, where each CAB1 is programmed into a dynamic latch as shown in Fig. 16b. The input signals to the two dynamic latches are 180 degree phase shifted, which is generated by a digital inverter. The forward signal path between two latches are implemented by a switch-less interconnect connecting two adjacent columns of the CAB matrix. The feedback between the output ports of

TABLE II
COMPARISON WITH PRIOR WORK

	Technology	Architecture	Operating Freq.	Area	Num. of CABs	Application	CAD
[2]	350 nm	FG-based	57 MHZ	9 mm^2	32	Receiver / Speech Processor	Simulink
[3]	130 nm	Switch-less	82 MHz	1 mm^2	7	Filter	-
[6]	2 µm	Switch-based	10 MHz	626 µm x 750 µm	40	Analog Arithmetic Operations / Filter	-
[7]	90 nm	Switch-less	500 Hz	-	27	Filter	-
[8]	350 nm	FG-based	18 MHz	84 mm^2	108	Analog-to-digital Conversion	Verilog / Matlab
[9]	350 nm	Switch-based	20 MHz	0.9 mm^2	25	Translinear Computing	-
[10]	350 nm	FG-based	200 KHz	9 mm^2	18	Translinear Computing	Verilog / Matlab
This Work	65 nm	hybrid	1.5 GHz	0.1 mm^2	36	Filter / Oscillator / Divider	Python / Ocean

D_1 and the input ports of D_2 is provided through the global feedback network. The results from the transient simulation of a frequency divider are provided in Fig. 17, which depicts four 100 MHz signals each 90 degree phase shifted.



(a) (b)

Fig. 16. Schematic representation of (a) the frequency divider configured with two CABs, where both CABs are programmed to implement differential dynamic latches, and (b) the implemented differential dynamic latch.

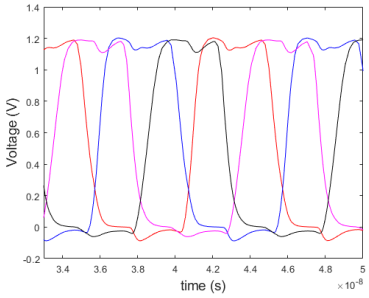


Fig. 17. Transient simulation of a divide-by-2 frequency divider with a 200 MHz input frequency. The four outputted signals are 90 degree phase shifted, with all four signals providing full voltage swing (1.2 V).

VI. COMPARISON WITH PRIOR FPAA

A comparison with prior FPAA topologies is provided through Table II. Metrics that are evaluated include the operating frequency, area, number of CABs, targeted applications, and software interface. In general, utilizing more routing switches increases the programming flexibility of the FPAA at the cost of lower operating frequency due to the parasitic impedance introduced by the switches. A switch-less interconnect improves the operating frequency of the circuits but limits the reconfigurability of the array due to the fixed connections between the CABs. The proposed FPAA architecture includes a hybrid interconnection network, where routing switches are implemented within the CABs and switch-less interconnects are utilized to form connections between the CABs. As compared to the floating-gate based topologies [2], the proposed FPAA occupies less area and operates at higher frequencies due to the use of fewer routing switches, while the flexibility of individual CABs is improved as compared to the completely switch-less architecture [3].

VII. CONCLUSION

In this paper, a novel FPAA architecture is proposed which includes a 6x6 CAB matrix implemented in a 65 nm CMOS process. The programmability of the FPAA is guaranteed by the routing switches within each CAB and the utilization of multiple CABs. The multi-CAB circuits implemented on the FPAA include a two-stage op amp, a lossy integrator, a ring oscillator, a second order biquad filter, and a frequency divider. The FPAA includes 36 CABs, 14 switch-less interconnects, and 498 routing switches that occupy an area of 0.1 mm^2. The configured two-stage op amp provides a DC gain of 37.8 dB and a 3-dB bandwidth of 60 MHz. The lossy integrator provides a tunable gain that ranges from 0 dB to 10 dB. Based on the number of implemented stages, the frequency generated by the ring oscillator ranges from 207 MHz to 478 MHz. For the configured biquad filter, the peak gain ranges from -9 dB to 8 dB. The divide-by-2 frequency divider provides 90 degree phase shifted signals for a maximum input frequency of 200 MHz.

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